Analysis of V_{on} Shift Phenomenon on Indium-Gallium-Zinc Oxide Thin-Film Transistors with Thermal-Induced Source/Drain Regions

Jiapeng Li, Lei Lu and Man Wong

Department of Electronic and Computer Engineering

The Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong

Abstract

Indium-Gallium-Zinc oxide thin film with seal cover above source/drain regions was found to efficiently creating homojunctioned TFTs with annealing process. However, the accompanying negative turn-on voltage (Von) shift, caused by ion diffusion in etch stopping (ES) layer, greatly degraded the device performance. To characterize and resolve the Von shift issues in thermal induced a-IGZO TFTs, the dependence of the device turn-on characteristics on cover material, cover thickness and ES thickness was investigated. As a result, we found that the ES thickness has the major impact on the drastic Von shift.

1. Introduction

Metal-oxide semiconductors, due to its transparency in the visible spectrum, relatively high carrier mobility and lower processing temperature, have received intense attention as very promising materials to replace amorphous Si (a-Si) in thin-film transistors (TFTs). Zinc oxide (ZnO) and its variants, such as indium-gallium-zinc oxide (IGZO), are the hottest metal-oxide materials which have already been applied in the modern display application[1].

We have developed a novel IGZO TFTs technology which covers the source/drain regions of a thin film transistor with gas-impermeable films like SiNx[2], Al_2O_3 or most of metals but exposes the channel region to the oxygen-enriched environment. Subsequent annealing process in an oxidizing atmosphere will maintain the channel at an intrinsic high resistivity stage (at least $10^4\Omega$.cm) but transform the S/D regions to relative lower ρ ($10^{-2}\Omega$.cm)[3]. The excellent conductive S/D regions, which benefit admirable contact with metal pad, are contributed to the defects aggregation resulted from thermally-induced dissociation of the IGZO. Nonetheless, the decomposed metal ions In^+, Ga^+, Zn^+ are found to diffuse into the etch stopping layer from SMIS result. The barged metal ions are supposed to cause the severe Von shift problem. Cover material, cover thickness and ES thickness are considered as the dominated factors in the structural configurations which control the whole ion migration process. Therefore, the influence of each parameter in thermal induced S/D IGZO TFTs is investigated.

2. Experimental Details

The schematic diagram of a thermal induced S/D IGZO TFT was shown in the inset of Fig. 1. A whole highly N-doped 4 inch Si substrate was used as the bottom gate. 50nm IGZO thin film was room-temperature sputtered above 100nm thermal oxide. The deposited ambience consisted of 10% oxygen (O_2) and 90% argon (Ar), with a total pressure of 3 mTorr and RF power 120W. Then IGZO thin film was patterned as active islands together with a protected oxide layer deposited at 300°C in a plasma-enhanced chemical vapor deposition (PECVD) reactor using tetraethylorthosilicate (TEOS) and O_2 as the source gases. Subsequently, a second TOES oxide layer was deposited to clad the active area just before covering the wafer with the gas-impermeable SiNy (PECVD) or Al_2O_3 (ALD) film. The channel region was defined with photolithograph and dry etching technology. The deposited SiO_x layer functioned as the protecting mask during active area patterning and etch stopping layer in the process of channel opening. The thickness of the ES SiO_x layer varied from 100nm to 200nm and the sealed cover thickness had three parameters of 20nm, 60nm and 100nm. The following O_2 annealing activation was carried out at 500°C for 30mins or 600°C for 20mins in Rapid Thermal Annealing (RTA) equipment. The characteristics of the fabricated TFTs after opening contact holes were measured by using an Agilent 4156C semiconductor parameter analyzer.

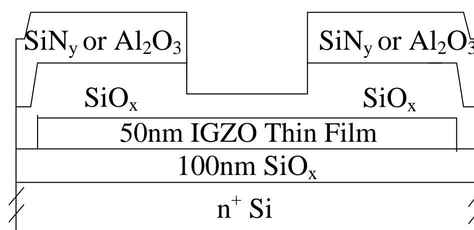


Fig. 1. The Cross-section of the thermal-induced S/D Indium-Gallium-Zinc Oxide Thin-Film Transistors

For the preparation of IGZO SMIS samples, 100nm IGZO was sputtered by using the same recipe mentioned above on the SiO_2 (5000A)/Si substrate. Then 100nm TOES oxide simulated as the ES layer was deposited followed by SiNx or Al_2O_3 covering. After the O_2 thermal activation at 500°C for 30mins, Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) was

employed for investigating ion diffusion in the ES layer. The cross-section of the IGZO SMIS samples was revealed in the Fig.2.

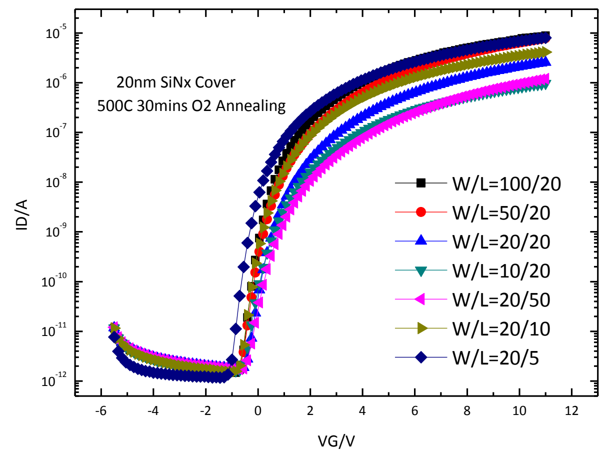
SiN_y or Al_2O_3 or None
100nm SiO_x
100nm IGZO
500nm SiO_x
Si Substrate

Fig. 2. The Cross-section of the IGZO SMIS Samples for investigation of ions diffusion in the ES layer

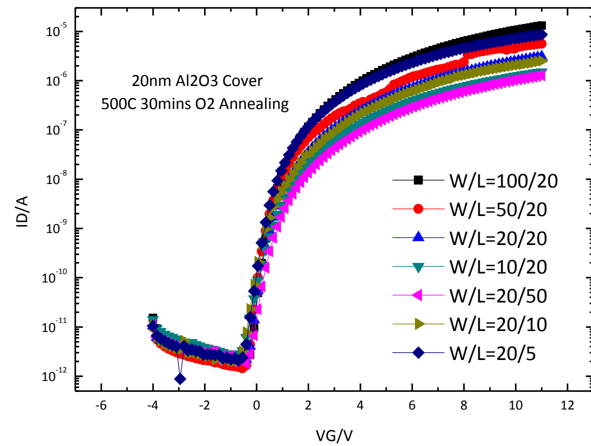
3. Results and Discussion

Fig. 3 shows the I_D-V_G transfer curve of TFTs with different sealed covers. The drain voltage is fixed at 5V and the thickness of both covers SiN_y and Al_2O_3 is 20nm. The etch stopping oxide layer thickness is 150nm (75nm+75nm). It can be seen from Fig. 3(a) and (b), both devices reveal good performance with the Von around -0.7V and excellent consistency for different W/L ratios. In other words, -0.7V can be regard as the reference value of Von. Very small negative Von shift has been observed when the channel length decreases from 50µm to 5µm which is easy to understand with the assumption that IGZO only dissociates under the sealed regions (S/D). Therefore, there is an ions diffusion process in the ES layer from unsealed regions to the unsealed. The short of channel, the more passive influence affected from charged ions in the ES layer above channel area. For short channel devices, less von shift is observed among those with Al_2O_3 cover. However, if aggressive annealing conditions are adopted, for the same W/L=20µm/20µm, devices with Al_2O_3 cover exhibits obvious smaller Von shift than the SiN_y covered devices even both Von shift is quite large. It is because that In^+ and Ga^+ ions are more likely to be absorbed by SiN_y than Al_2O_3 film observed from SIMS result. Therefore if no saturation of ion diffusion in ES layer is reached, SiN_y cover can drag more ions into the ES layer during the same annealing time which results in the severe Von shift problem. The I_{off} difference in Fig. 3(c) comes from the gate leakage which is determined by the fluctuant gate dielectric quality. The lower Ion under higher temperature annealing is supposed to result from the higher S/D resistance.

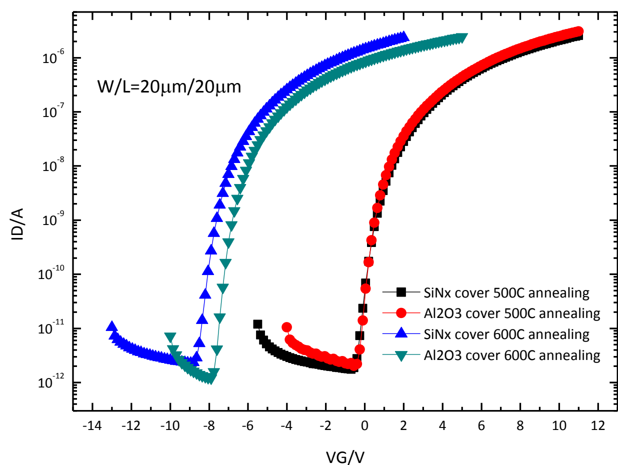
Fig. 4 demonstrates the dependence of Von shift on the sealed SiNx cover thickness. 200A, 600A and 1000A PECVD SiNx layers are employed as the cover respectively. According to the previous transfer curve in Fig. 3(c), 500℃ O_2 annealing in RTP for 30mins will not lead to drastic Von shift, the corresponding devices turns on at about -0.7V gate voltage regardless of different thickness. When the annealing temperature increases to 600℃, obvious Von negative shift up to -9V occurs on all TFTs. Very little difference of Von between devices with different thick SiN_y covers indicates that the function of sealed cover is not affected by thickness. The domination of ion diffusion does not take place in the interface of SiN_y and SiO_x. It may be controlled by ion migration in the etch-stopping layer or the dissociation process in the IGZO thin film. Further investigation about the influence of ES thickness is shown in the Fig. 5.



(a)



(b)



(c)

Fig. 3. (a) I_D-V_G curve of thermal-induced S/D IGZO TFTs with 200A SiNx cover, 500℃ annealing for 30mins; (b) I_D-V_G curve of thermal-induced S/D IGZO TFTs with 200A Al_2O_3 cover, 500℃ annealing for 30mins; (c) I_D-V_G curve of thermal-induced S/D IGZO TFTs under different annealing conditions

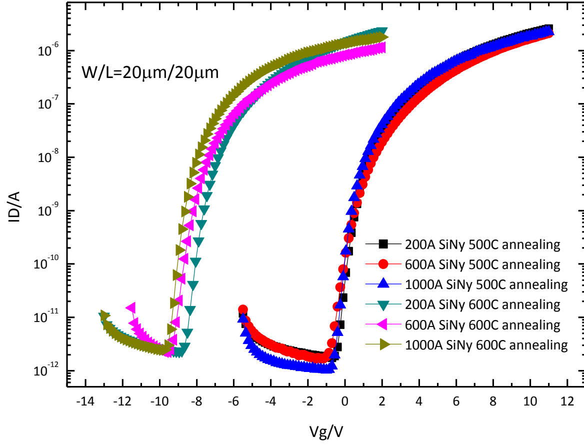


Fig. 4. I_D-V_G curve of thermal-induced S/D IGZO TFTs with different SiN_y cover thickness

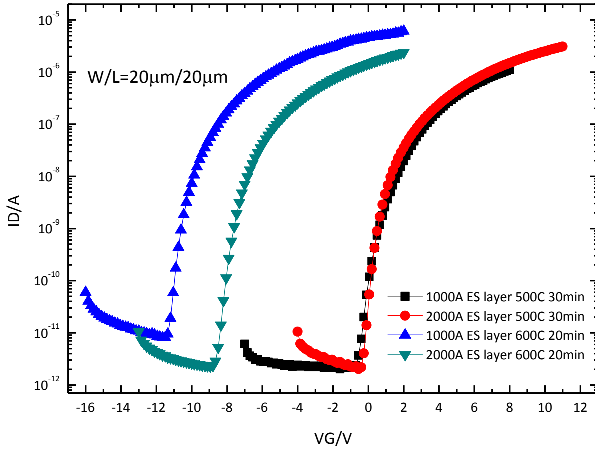


Fig. 5. I_D-V_G curve of thermal-induced S/D IGZO TFTs with different ES layer thickness

Consistent with previous studies, gentle annealing at 500℃ O_2 annealing for 30mins has not brought Von shift. 600℃ annealing for 20mis produces -9V and -11V for 2000A ES layer and 1000A ES layer devices relatively. And distinct device performance yields during annealing process which is related with channel oxidation and S/D region ions production and diffusion. It is guessed that the thicker of SiO_x layer, the more oxygen in the oxide can be provided into the IGZO film S/D regions under anaerobic environment. Then less IGZO dissociation will happen for 2000A ES layer device than 1000A ones. Thicker ES layer can also hinder the ion diffusion in the vertical direction as ions were attracted by the sealed cover which indirectly brings about sluggish in the horizontal direction. All the possibility will lead to the subdued Von shift phenomenon.

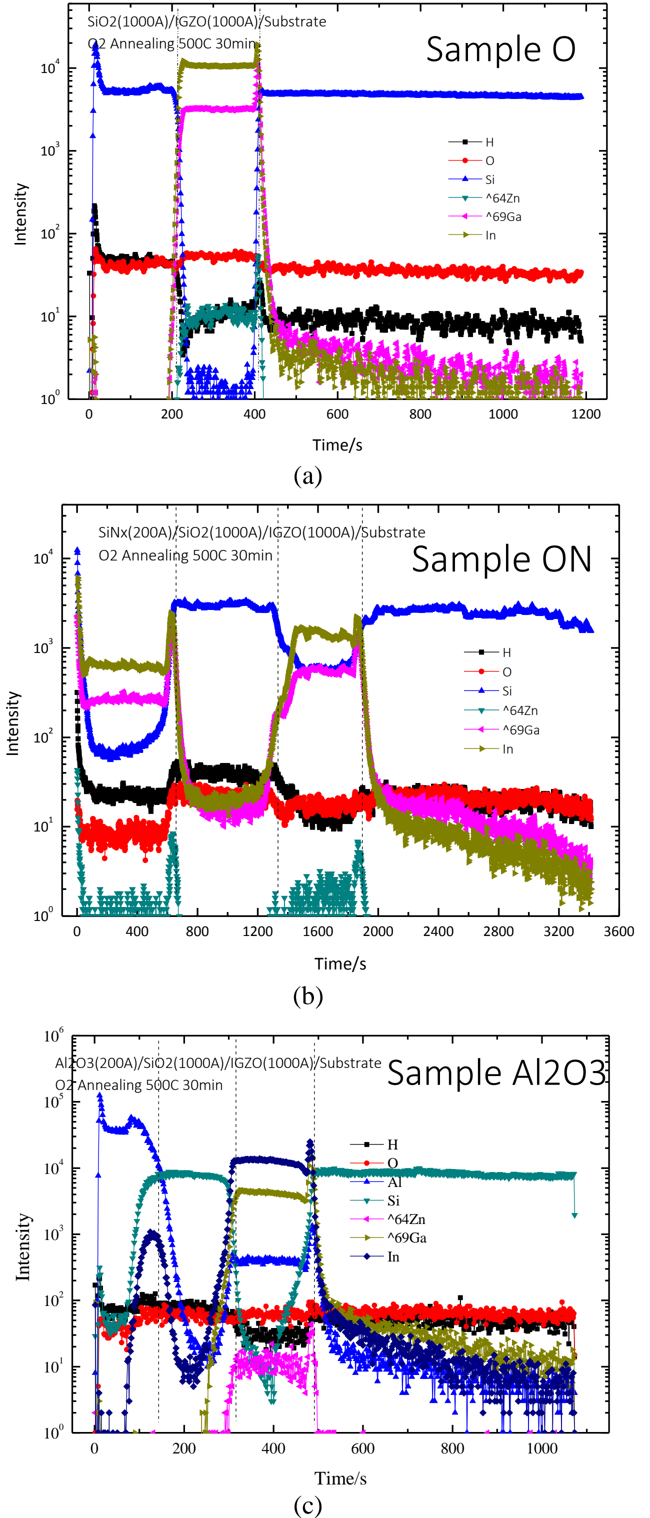


Fig. 6. (a) SMIS result of IGZO thin film covered with SiO_2 after annealing; (b) SMIS result of IGZO thin film covered with SiO_2 and SiNx after annealing; (c) SMIS result of IGZO thin film covered with SiO_2 and Al_2O_3 after annealing

Fig. 6 shows the SMIS results of IGZO thin film covered with different configuration after O_2 annealing at 500C for 30mins. The x axis Time/s means the measurement time which corresponds to the depth in the sample. By analyzing the element, it is easy to divide each layer of sample configuration which is marked with imaginary line. From Fig. 6(a), as IGZO was covered with permeable oxide, O_2 annealing will not give rise to IGZO decomposition, therefore no metal ions are observed in the SiO_2 layer. And the intensity of metal In, Ga, Zn almost keeps uniform across the IGZO layer. Conversely, annealing under the sealed covers will cause the IGZO dissociation, as a result the intensity of metals in the IGZO layer fluctuates. Especially for the sample ON which IGZO was covered with SiO_2 and SiNx, there is large amount of In+ and Ga+ ions diffuse across through the oxide layer and gather in the SiNx layer. Accordingly, the Al_2O_3 cover also attracts In+ ions and results in an ions intensity gradient in the oxide layer. However the ions diffusion with Al_2O_3 cover is much weaker than SiNx which is determined by ions solubility in these covers. The SMIS results verify the production and diffusion of metal ions, and can be thought as an indirect examination of previous study and supposition.

4. Conclusion

Under investigating the dependence of Von shift on cover material, cover thickness and ES thickness, it is found that after IGZO film dissociating under high temperature annealing and anaerobic environment, the ES thickness plays a significant role in the ion diffusion compared with the sealed cover materials and thickness in the device configuration. Attention must be paid to look for the appropriate sealed cover which has slightly attracting effect of In^+, Ga^+ ions. Increasing the thickness of ES layer is a decent choice for eliminating Von shift as well. It is anticipated that when the much thicker ES layer were introduced into the thermal induced S/D IGZO TFTs, it can decrease the Von shift and also function as the passivation layer to package the devices. It should be mentioned that reasonably controlling annealing temperature will be the most effective method to avoid the sever Von shift.

References

1. Fortunato, E., et al. "Recent advances in ZnO transparent thin film transistors." Thin solid films 487.1 (2005): 205-211.
2. Lu, Lei, and Man Wong. "A Bottom-Gate Indium-Gallium-Zinc Oxide Thin-Film Transistor With an Inherent Etch-Stop and Annealing-Induced Source and Drain Regions." Electron Devices, IEEE Transactions on 62.2 (2015): 574-579.
3. Lu, Lei, Jiapeng Li, and Man Wong. "A comparative study on the effects of annealing on the characteristics of zinc oxide thin-film transistors with gate-stacks of different gas-permeability." (2014): 1-1.