Achievement of High-Performance and Environmentally Stable TFTs by Introducing Hybrid-Phase Microstructure into InSnZnO Channels

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ABSTRACT

A novel hybrid-phase microstructure are introduced into InSnZnO thin films, where a number of nanocrystals are embedded in an amorphous matrix. Following the study on microstructural and electrical properties of thin films, the corresponding staggered bottom- and top-gate thin-film transistors with optimal channels are both fabricated and exhibit a fairly high and uniform electrical performance, especially in field-effect mobility and subthreshold swing. In addition, such devices are also proven to be air-stable owing to in situ passivation of hybrid-phase microstructural InSnZnO channels.

1. Introduction

Recently, metal oxide (MO) semiconductors have drawn great attention as TFT channels, and these MO thin-film transistors (TFTs) possess many promising advantages, such as reasonable electrical performance and high optical transparency, low processing temperature and production costs as well [1,2]. Since reported by Hosono et al. in 2004 [3], amorphous indium-gallium-zinc oxide (a-IGZO) promptly became the most prevalent multicomponent MO material, and its electrical properties are not deteriorated too much in spite of the atomic disorder. However, with the advancement of next-generation active-matrix (AM) displays towards large area, ultra-high definition (UHD) display, and system on panel (SoP), a-IGZO seems still insufficient to fulfill the requirements of TFTs for higher mobility [4-5]. As the fundamental binary MO material, ZnO is attractive with medium electrical performance, and its earth-abundance offers potential opportunities in low-cost applications. But, the pristine polycrystalline ZnO (pc-ZnO) TFTs always suffer from native defects (such as oxygen vacancies (VO), dangling states) and grain boundaries (GBs), which result in severe instability issues and required further modifications [1]. On the other hand, it is always controversial on whether the amorphous phase overweighs the nanocrystalline phase in MO semiconductors, in particular after the amorphous oxide semiconductors (AOS) mobility limits are proposed [5]. For most MO TFTs, their best performance is actually obtained at the boundary between the amorphous and crystalline phases.

In this paper, a novel hybrid-phase microstructure with nanocrystals blended in amorphous phase was introduced into InSnZnO thin films for the first time. Then, the corresponding bottom- and top-gate TFTs were both successfully fabricated and exhibited remarkable electrical performance with device uniformity comparable to AOS TFTs. Moreover, the devices even without any passivation were found to be air-stable, and in-situ passivation of channels is given to explain such phenomenon.

2. Deposition and Properties of Films

As known, the sputtered ITO and ZnO thin films are generally polycrystalline. When ITO and ZnO are blended together using dc and rf sputtering power, respectively, a novel hybrid-phase microstructure is found in the deposited thin films, where parts of ITO/ZnO grains survive in nanocrystalline phase and are embedded in an amorphous matrix. In Fig. 1a, the X-ray diffraction (XRD) spectra display a quite weak and wide peak between ITO (222) peak and ZnO (002) peak. According to Scherrer's equation, the grain size derived is about 1.5 nm, indicating the existence of nanocrystals inside the co-sputtered thin films. The microstructure was further probed using a high resolution transmission electron microscope (HRTEM). It can be seen that the columnar nanocrystals with clear lattice fringes are sparsely distributed in the amorphous matrix, so the grain boundaries are diluted (Fig. 1b). Different from other amorphous InSnZnO films, it is believe that the inherent hybrid-phase microstructure will also make a great contribution to TFTs with high electrical performance and stability especially in comparison with the pc-ZnO and a-IGZO TFTs.

Since the conductivity of ITO and ZnO are both sensitive to the amount of V_O inside thin films, the

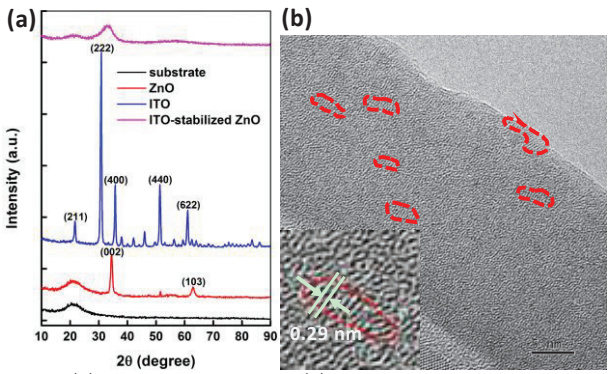

Fig. 1. (a) XRD spectra and (b) cross-sectional HRTEM image of hybrid-phase microstructural InSnZnO thin films.

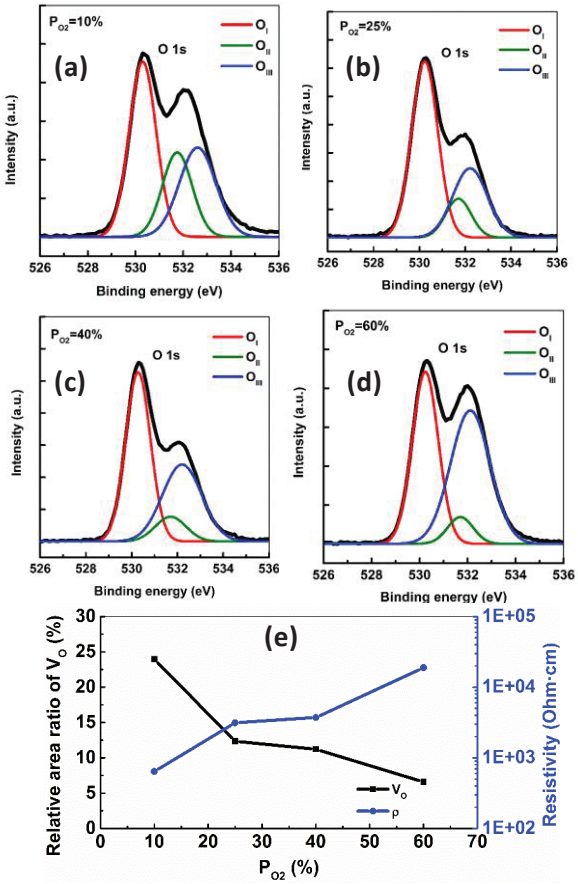

Fig. 2. XPS O 1s spectra of hybrid-phase microstructural InSnZnO thin films co-sputtered with P_{O2} of (a) 10%, (b) 25%, (c) 40% and (d) 60%; (e) the relative area ratio of V_O and resistivity of thin films as a function of P_{O2}.

oxygen partial pressure ratio ($P_{O2}=O_2/(Ar+O_2)$) is regarded as one of most important parameters to affect the electrical properties of co-sputtered films. To understand the relationship more clearly, X-ray photoelectron spectroscopy (XPS) was used to analyze the chemical states of oxygen in the deposited thin films. As shown in Fig. 2a-2d, the XPS spectra of O 1s peak can be divided into three peaks O_I, O_{II}, O_{III}, and further fitted as a Gaussian distribution. Theoretically, the O_I, O_{II} and O_{III} peak are relevant to the oxygen bonded in oxide lattices (In-O, Sn-O and Zn-O), oxygen deficiencies in lattices (such as V_O) and chemisorbed oxygen (such as the bonded oxygen in hydroxyl groups), respectively. These peaks are correspondingly centered in the vicinity of 530.2 eV, 531.6 eV and 532.2 eV. The symmetric variations in Fig. 2(e) imply that P_{O2} can regulate the amount of V_O and indirectly manipulate the electrical conduction of InSnZnO thin films. When P_{O2} rises from 10% to 60%, the relative area ratio of V_O decreases to only 6.58%, and the resistivity differs by nearly two orders of magnitude when oxygen is in insufficient and excess status.

3. Device Fabrication

With hybrid-phase microstructural InSnZnO channels, both staggered bottom-gate and top-gate TFTs were fabricated. The bottom-gate device started on 4-inch heavily doped n-type silicon wafers, which were coated by 120-nm-thick thermal oxide on the front surface. 50-nm-thick InSnZnO channels were deposited on SiO_2/Si substrates using magnetron co-sputtering the ITO (90 wt% In_2O_3 and 10 wt% SnO_2) and ZnO target at room temperature. In order to obtain TFTs with optimal electrical performance, various sputtering conditions including P_{O2} and dc power (P_{DC}) are attempted. Next, the active channels were patterned using conventional photolithography and etched in diluted hydrofluoric acid. The channel width and length were 90 μm and 45 μm, respectively. After photoresist stripping and drying, a lift-off method was performed to form Al source and drain (S/D) electrodes, which was deposited by DC magnetron sputtering. Finally, the devices were subjected to thermal annealing at 300°C in air. The electrical characteristics of devices were measured in the probe station using a semiconductor parameter analyzer (Agilent 4156C).

Based on the co-sputtering conditions employed in the optimal bottom-gate TFTs, the staggered top-gate TFTs were then fabricated. The substrates were 4-inch p-type silicon wafers coated with 500-nm-thick thermal oxide. 80-nm-thick ITO was formed as S/D electrodes by lift-off technique at first. The InSnZnO channels were then deposited with P_{O2} of 40% and P_{DC} of 120 W, and patterned into active islands by wet etch. Next, 150-nm-thick PECVD-SiO_2 gate dielectric and 200-nm-thick Al gate electrode deposition was performed in sequence, followed by dry etch processes. The devices were also annealed at 300°C in air, and the whole processes were conducted within 300°C.

4. Results and Discussion

Fig. 3(a) reveals the transfer curves with various sputtering P_{O2} under a constant dc and rf power (120 W

dc and 150 W rf). It is noted that there exists a dramatic threshold voltage (V_{th}) shifts from -35.85 V to -0.75 V when P_{O2} initially rises. This is consistent with the sharp decrease in relative area ratio of V_O (Fig. 2). However, the field-effect mobility (μ_{fe}) always maintains at relatively high values (>20 $cm^2 V^{-1} s^{-1}$). According to Adler's percolation conduction model, μ_{fe} generally increases with the rise of carrier concentration, because more carriers can reduce the potential difference between Fermi level and percolation potential barriers. On the other hand, if the intrinsic height of percolation potential barriers is low, carriers can also transport with less impedance. For the InSnZnO thin films with hybrid-phase microstructure, the height reduction of percolation barriers is possibly provided by the ordered atomic arrangement within nanocrystals, diluted grain boundary density, and 5s orbital overlaps of In/Sn cations in the amorphous matrix. Fig. 3(b) shows an obvious change in electrical performance of devices when P_{DC} climbs beyond 60 W. One plausible explanation is that the channels are dominated by pc-ZnO and fail to exhibit the advantages in hybrid-phase microstructural InSnZnO thin films. Above all, the optimal devices are obtained when P_{O2} and P_{DC} are set as 40% and 120 W, respectively. The key electrical parameters of corresponding bottom- and top-gate TFTs are listed in Table 1, and their transfer and output curves are plotted in Fig. 4.

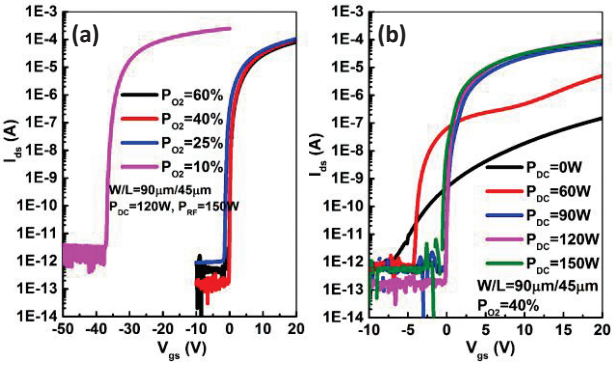

Fig. 3. Transfer curves of hybrid-phase microstructural InSnZnO TFTs with various (a) P_{O2} and (b) P_{DC}.

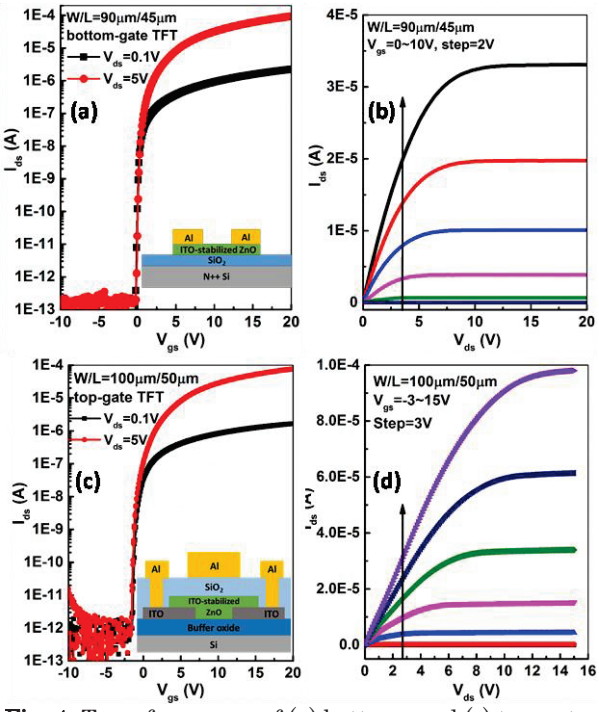

Fig. 4. Transfer curves of (a) bottom- and (c) top-gate TFTs; output curve of (b) bottom- and (d) top-gate TFTs.

Table 1. Key electrical performance of bottom- and top-gate TFTs with the optimal hybrid-phase microstructural InSnZnO channels

	Bottom-gate	Top-gate
V_{th} (V)	0.46	-0.65
μ_{fe} (cm^2/Vs)	26.08	19.10
On-off ratio ($\times 10^8$)	10.9	1.61
SS (V/decade)	0.089	0.115

Fig. 5 shows the spatially uniformity of bottom-gate TFTs over a 4-inch silicon wafer, which was comparable to AOS TFTs. Apart from the enhanced device behaviors, it is clearly seen that all the transfer curves shift within a rather narrow range. This is because the grain size of nanocrystals inside is no more than 2 nm. When involved in TFTs with micrometer scaled channel length, these nanocrystals look quite small and sparse, and the diluted grain boundaries can be almost negligible.

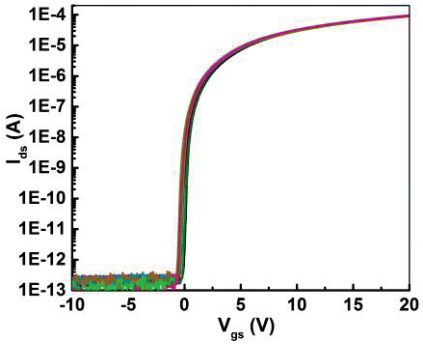

Fig. 5. Transfer curves of 15 bottom-gate hybrid-phase microstructural InSnZnO TFTs, which are uniformly distributed over a 4-inch silicon wafer.

Furthermore, Fig. 6 illustrate the excellent environment stability of TFTs, even for the unpassivated bottom-gate devices with backsurface exposed in air. The V_{th} of unpassivated bottom-gate devices only drops from about 0.5 V to below zero within the first day, then achieves a dynamic equilibrium for a long period, which are much air-stable than those pristine pc-ZnO and a-IGZO TFTs. Such phenomenon can be explained by in situ passivation of channels. Specifically, ZnO-based nanocrystals inside can be encapsulated by the amorphous InSnZnO matrix, which is less sensitive to

the ambient. Therefore, it suppresses the ambient chemisorption effects at the backsurface and grain boundaries of ZnO.

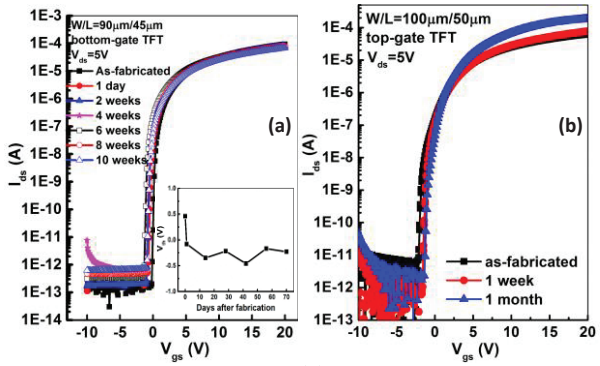

Fig. 6. The air stability of (a) unpassivated bottom- and (b) top-gate TFTs with hybrid-phase microstructural InSnZnO channels.

5. Conclusions

A novel hybrid-phase microstructure was introduced in InSnZnO thin films for the first time, where nanocrystals were embedded in an amorphous matrix. The microstructural and electrical properties of thin films were then studied. Afterwards, both corresponding bottom- and top-gate TFTs were fabricated and exhibited remarkable electrical performance and uniformity. At last, as a unique merit of the hybrid-phase microstructure, in situ passivation of channels was pointed out to explain the excellent environment stability of devices.

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