Fabrication of High-Performance Bridged-Grain Polycrystalline Silicon Thin-Film Transistors with Laser Interference Lithography Technology

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ABSTRACT

Laser interference lithography (LIL) technology was introduced to pattern periodic submicron bridged-grain (BG) structures in the fabrication of BG-TFTs. The relationship between LIL exposure energy density and device electrical performance was investigated, and it was found that 60 mJ/cm^2 is the optimal parameter, in order to achieve enhanced TFT electrical performance while maintaining relatively good uniformity.

1. INTRODUCTION

Low-temperature polycrystalline silicon (LTPS) thin-film transistor (TFT) is regarded as one of the most promising candidates for backplane technology to realize high-performance active-matrix flat panel displays (FPDs). In LTPS technology, due to the better crystalline quality of recrystallized poly-Si film compared with directly deposited one, processes such as excimer laser annealing (ELA), solid phase crystallization (SPC) and metal-induced crystallization (MIC) are proposed to convert a-Si into polycrystalline phase with fewer defects. However, this suffers from high density and random distribution of grain boundaries (GBs), which will result in non-uniform and degraded electrical performance of TFTs across the panel. So it is necessary to mitigate the effect of GBs.

In this paper, a BG structure is employed in MIC LTPS TFTs to boost the electrical performance and its corresponding uniformity, which can link neighbor grains and form many submicron spacing. Besides, in order to form this kind of special structure, laser interference lithography (LIL) technology is introduced into the patterning process, followed by investigating the relationship between LIL exposure energy density and eventual device electrical performance. Furthermore, considering another factor, namely uniformity, an optimal LIL exposure energy density is defined.

2. FORMATION OF BG STRUCTURES WITH LIL

2.1 BG Structures

A BG structure (Figure 1) is made up by a series of heavily doped parallel BG regions in the active channel, which are perpendicular to drain current direction. Across the BG regions, neighbor grains are linked and most GB barriers can be suppressed. In other words, when the carriers enter into the conductive BG regions, they are able to choose those shortcuts provided by BG lines, so a large number of GB barriers and traps along the transport path can be avoided, resulting in lower V_{th}, steeper SS and higher mobility. Besides, the BG lines divide a long poly-Si active channel into many submicron spacing. Consequently, in the ON-state, the short channel effect is helpful to further reduce V_{th} and increase carrier mobility. Meanwhile, similar to a multiple-gate device, the heavily doped regions can form depletion junctions with their neighbor intrinsic material. This will partially distribute the high electric field near the drain, leading to lower gate induced drain leakage (GIDL) current in the OFF-state. It has been proved that compared with conventional LTPS TFTs, all of key parameters including V_{th}, SS, field-effect mobility, on-off ratio and leakage current in BG-TFTs can be improved [1-3]. However, parameters of BG lines such as number, size and implantation conditions, which can bring the maximum optimization, have not been sufficiently investigated yet.

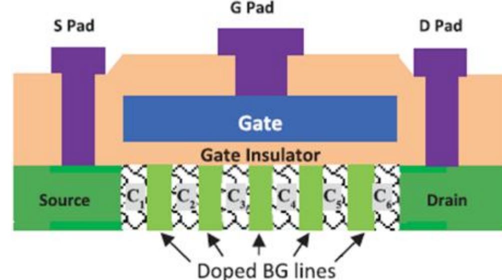


Figure 1. Cross-sectional schematic of a BG-TFT, which owns highly conductive BG lines in active channel to provide shortcuts for carriers [1].

2.2 LIL Technology

In order to pattern the periodic submicron BG structure, technologies like photolithography [1], laser interference lithography [2] and nanoimprint lithography [3] have been introduced. However, considering practical manufacture, additional fabrication processes mean inevitably extra costs. For example, there is no specific photolithographic stepper available for BG lines patterning. In this sense, LIL technology is a relatively preferable choice, because it is maskless and controllable for interference pattern period.

As shown in Figure 2, the LIL system is based on the holographic interference technique [4], and the photosensitive layer is exposed by the spatially periodic interference fringes, which are formed by two coherent laser beams. The interference pattern period follows the equation: $\Lambda=\lambda/2\sin\frac{\theta}{2}$, where λ is the laser wavelength and θ is the angle between two laser beams [4-6]. Since the laser source in this paper is an ultraviolet argon-ion laser with a wavelength of 363.8 nm, for 1-μm pattern period, the corresponding angle θ is calculated as 20.96°.

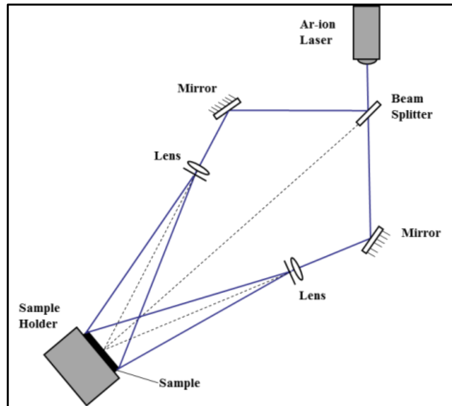
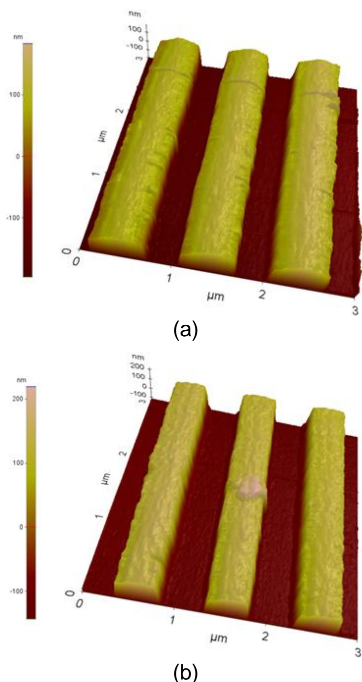


Figure 2. Schematic of LIL system used (also called holographic interference system).



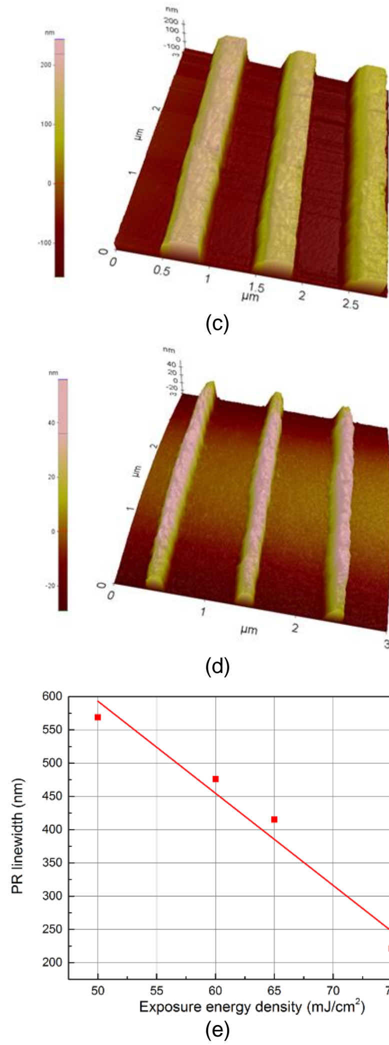


Figure 3. AFM images of the exposed grating structures after LIL with the exposure energy density of (a) 50 mJ/cm^2, (b) 60 mJ/cm^2, (c) 65 mJ/cm^2 and (d) 75 mJ/cm^2. (e) Plot of the remaining PR width (covered region) versus the exposure energy density and its corresponding fitted curve after LIL.

3. DEVICE FABRICATION

The process started from low-pressure chemical vapor deposition (LPCVD) of 45-nm-thick a-Si on 4-inch p-type silicon wafer coated with 500-nm-thick thermal oxide. Then, nickel silicide was sputtered on the surface of a-Si layer, which induced conversion from a-Si film to poly-Si film by following nitrogen annealing at 600 °C for 10 h. After recrystallization, NiSi was removed by sulfuric acid cleaning. Next, antireflection coatings (ARCs) and positive photoresist (PR) AZ1075 were spin-coated on the surface of poly-Si active layer in sequence, and then PR was patterned into gratings with a period of 1 μm using LIL technology. Since the aspect ratio (exposed : covered) would vary with the exposure energy (Figure 3), the energy density adopted in this paper were 0 mJ/cm^2, 50 mJ/cm^2, 60 mJ/cm^2, 65 mJ/cm^2 and 75 mJ/cm^2, to investigate exposure energy density's influence on electrical performance of eventual devices and find out the optimized parameter. After hard-baking,

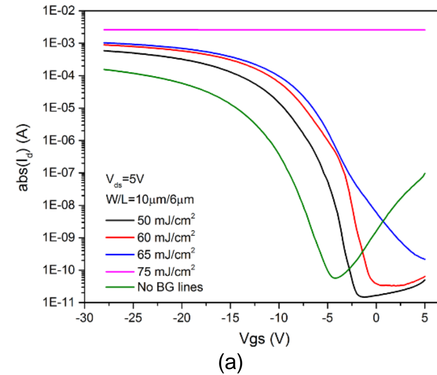
boron (B) implantation into the exposed regions was carried out with a dosage of 2×10^{15} /cm^2 and an energy of 23 keV. After ARC and PR removal, the BG lines were formed in the active channel, and no extra dopant activation process was needed. Then, the poly-Si layer was pattern into active islands using dry etch, followed by 50-nm-thick SiO_2 deposition using LPCVD, and this LTO served as gate dielectric. Afterwards, a 300-nm-thick aluminum (Al) was deposited and patterned as gate electrodes, while source and drain electrodes were formed by self-aligned B implantation with a dosage of 4×10^{15} /cm^2 and an energy of 25 keV. Subsequently, 500-nm-thick LTO as a passivation layer was deposited and contact holes were defined. A 700-nm-thick Al-1%Si layer was then sputtered and patterned as testing pads. Finally, the forming gas annealing (FGA) was performed at 420 °C for 30 min. During FGA process, the dopants in source/drain and BG regions could be activated simultaneously.

4. RESULTS AND DISCUSSION

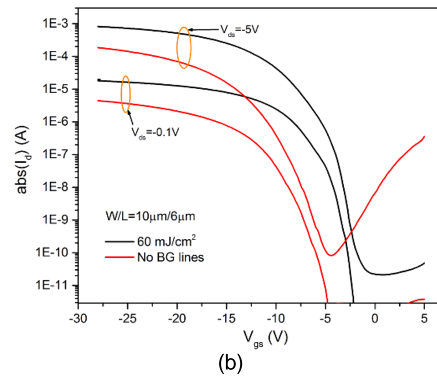
Table 1 lists all key electrical parameters of BG-MIC-TFTs with different LIL exposure energy density. Here, V_{th} is defined as V_{gs} when $|I_d|$ reached W/L$\times10^{-7}$ A at V_{ds}=-0.1 V, and the on-off ratio is the ratio of maximum and minimum value of $|I_d|$ at V_{ds}=-5 V. Besides, GIDL current is equal to $|I_d|$ at V_{gs}=5 V and V_{ds}=-5 V, divided by W. Figure 3 shows that with the increase of LIL exposure energy density, the exposed fraction also climbs, which indicates that the BG regions become larger whereas the separated submicron spacing gets shorter. Therefore, benefiting from the short channel effect, devices with higher LIL exposure energy density show lower V_{th} and higher μ_{fe}, resulting in larger ON-state current. Meanwhile, the high leakage current related to the short channel effect is overcome by the multiple junctions and varies slightly, so the on-off ratio rises overall. In addition, due to longer shortcuts provided by wider BG lines, μ_{fe} can be further increased. However, considering the lateral scattering of B dopants during implantation process, it is confirmed that too high LIL exposure energy density is not preferable, because shorter BG line spacing caused by over-exposure will make TFT active channel more conductive, and lose switch behavior eventually. The transfer characteristics of BG-MIC-TFTs with different LIL exposure energy density are shown in Figure 4. According to Figure 4(a) and Table 1, it can be found that the TFTs are operated gradually from obvious enhancement mode towards depletion one. In particular, for the sample exposed under 75 mJ/cm^2, BG lines are shorted and all devices are out of use.

Table 1. Average electrical performance of BG-MIC-TFTs with different LIL exposure energy density

LIL exposure energy density (mJ/cm^2)	0	50	60	65	75
Aspect ratio (Exposed : Covered)	N/A	~0.432: 0.568	~0.525 :0.475	~0.575 :0.425	~0.779 :0.221
V_{th} (V)	-9.52	-6.04	-5.08	-1.87	N/A
μ_{fe} (cm^2/V • s)	23.51	74.49	104.51	135.55	
On-off ratio ($\times10^7$)	0.297	3.90	4.21	5.36	
GIDL (pA/μm)	7480	5.65	33.3	50600	

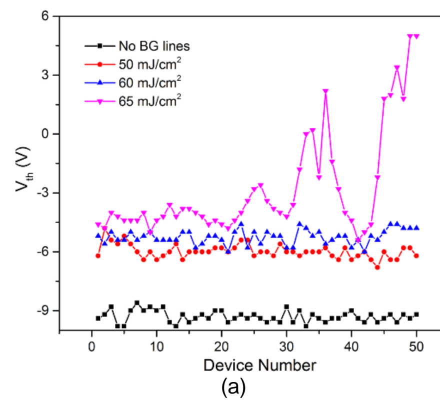


(a)



(b)

Figure 4. (a) Transfer characteristics of BG-MIC-TFTs with different LIL exposure energy density. (b) Transfer characteristics of MIC-TFTs without BG lines and with BG lines exposed under the optimized LIL energy density.



(a)

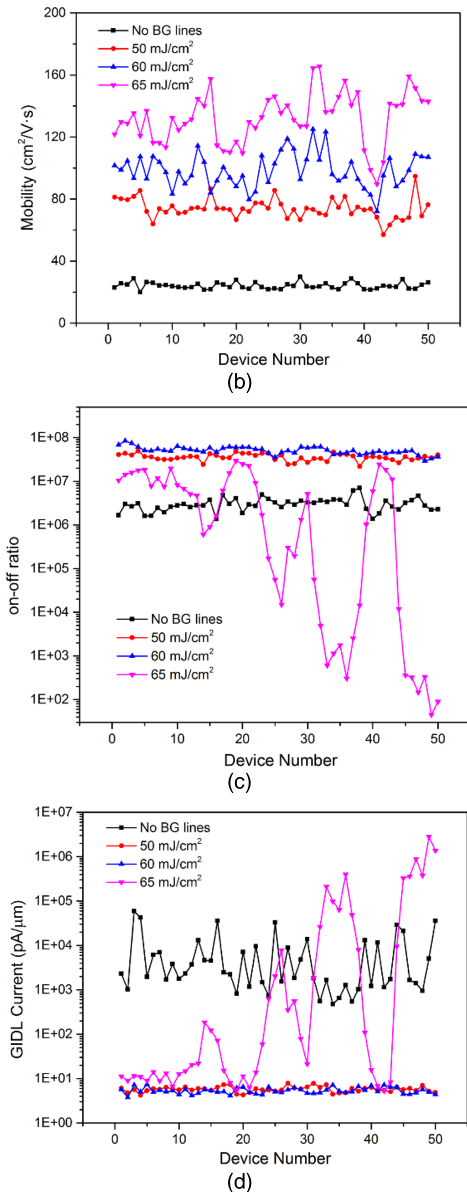


Figure 5. Electrical performance uniformity for 50 randomly distributed MIC-TFTs without BG lines and with BG lines exposed under different LIL energy density. (a) V_{th}, (b) field-effect mobility, (c) on-off ratio and (d) GIDL current.

On the other hand, Figure 5 shows that only if the LIL exposure energy density is set in a reasonable range (no more than 60 mJ/cm^2 in this paper), TFT electrical performance uniformity can be maintained, and even improved in terms of parameters such as on-off ratio and GIDL current. Thus, it is not LIL technology with proper exposure but other LTPS technologies that should be responsible for the performance variation. However, since the spots of two incident laser beams in LIL own Gaussian-like power distribution, further LIL exposure energy density increase will result in greater power variation among inference fringes, which will make a remarkable contribution to TFT electrical performance non-uniformity.

Above all, in view of both device electrical performance and its corresponding uniformity, it is believed that 60 mJ/cm^2 is a preferable LIL exposure energy density choice in this paper. Firstly, the fabricated BG-MIC-TFTs exhibit enhanced electrical performance with an average threshold voltage V_{th} of -5.08 V, on-off ratio of 4.21×10^7 and GIDL current of 33.3 pA/μm. Notably, compared with MIC-TFT without BG lines, the field-effect mobility μ_{fe} increasingly grows from 23.51 cm^2/V • s to 104.51 cm^2/V • s, as predicted. The comparison of transfer characteristics are shown in Figure 4(b). Meanwhile, the electrical performance uniformity for 50 randomly distributed BG-MIC-TFTs with a LIL exposure energy density of 60 mJ/cm^2 is also comparable to that for MIC-TFTs without BG lines.

5. CONCLUSIONS

The BG structure is effective to improve the electrical performance of LTPS TFTs, and the LIL technology adopted in BG structure patterning is a promising choice because it is maskles, controllable for interference pattern period and large-area applicable. Furthermore, considering the relationship between LIL exposure energy density and eventual device performance investigated, in addition to electrical performance uniformity, it was found that 60 mJ/cm^2 is an optimal LIL exposure energy density to achieve enhanced TFT electrical performance while maintaining relatively good uniformity.

ACKNOWLEDGEMENT

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