A Bottom-Gate Indium-Gallium-Zinc Oxide Thin-Film Transistor With an Inherent Etch-Stop and Annealing-Induced Source and Drain Regions

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***Abstract*— The resistivity of an indium–gallium–zinc oxide (IGZO) thin film was found to depend on not only the conditions of its thermal annealing but also the oxygen-permeability of the cover film during the heat treatment. Based on this observation, a technology for constructing a bottom-gate IGZO thin-film transistor with annealing-induced source and drain (S/D) regions is proposed and demonstrated. The S/D and channel regions with this device architecture are capped, respectively, by impermeable and permeable covers. During a subsequent heat treatment in an oxidizing atmosphere, the resistivity of the S/D regions is greatly reduced; while the channel region, being exposed to the oxidizing atmosphere through the permeable cover, retains its highly resistive character. The permeable cover protects the channel region by serving additionally as an inherent back-channel etch-stop during the etching of the impermeable cover. No patterning is needed to realize this etch-stop, implying a lower manufacturing cost.**

***Index Terms*— Annealing, cover, defect, indium–gallium–zinc oxide (IGZO), permeability, resistivity, thin-film transistor (TFT).**

I. Introduction

INDIUM–GALLIUM–ZINC oxide (IGZO) is a popular candidate [1] for replacing the silicon-based materials for constructing thin-film transistors (TFTs), particularly in flat-panel displays [1], [2]. Like many other semiconductors, it can be turned into an effective conductor using extrinsic dopants, such as hydrogen [3], [4] or phosphorus [5]. For IGZO and a host of similar metal-oxide semiconductors, their resistivity (ρ) also depends on the relative amount [6] and the binding states [7] of their oxygen constituents, such as the oxygen-related point defects [8], [9]. It is for this reason that IGZO can be made an effective conductor by either plasma treatment [3], [10], [11], or thermal annealing [7], [8].

The dependence of the ρ of sputtered IGZO thin films, both bare and capped, on the annealing atmosphere, time, and temperature was systematically studied and compared. This investigation was motivated by a recent report [12] that the ρ of zinc oxide (ZnO), a metal oxide from which IGZO is derived, was controlled by not only the process conditions but also the cover configurations of the ZnO during the annealing. Such behavior of ZnO has been attributed to the spontaneous generation and annihilation of donor-like defects [12]. In the present investigation, the lowest ρ was obtained for an IGZO sample annealed with an oxygen-impermeable cover made of silicon nitride (SiN_y) deposited using a plasma-enhanced chemical vapor deposition (PECVD) process; while a more complicated annealing effect was observed for the IGZO capped with an oxygen-permeable PECVD silicon oxide (SiO_x). The resulting ρ is either comparable to or lower than that of IGZO doped with extrinsic dopants [3]–[5] or intrinsic donor-like defects [7], [8], [10], [11].

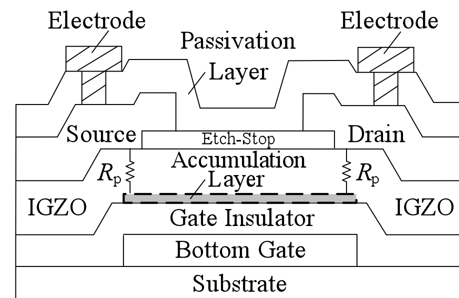

Fig. 1. Schematic cross section of an inverted-staggered TFT, indicating the location of a patterned etch-stop and the presence of the parasitic resistance R_p.

In the inverted-staggered architecture popularly used for an IGZO TFT [1], [2], [13] (Fig. 1), heterojunction contacts are formed between the source and drain (S/D) conductors and the intrinsic IGZO channel layer. Such contacts, if improperly constructed, may exhibit nonohmic behavior [14], [15]. Furthermore, a separately patterned back-channel etch-stop layer is sometimes employed to protect the channel from the etch used to define the S/D regions. Inherent in this structure is also a parasitic resistance (R_p) across the thickness of the channel layer [14]. This layer is typically undoped, hence highly resistive.

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Based on the observed dependence of the ρ of IGZO on the coverage configuration and the annealing atmosphere, a technology is proposed and demonstrated for constructing a TFT with annealing-induced rather than separately deposited [1], [2], [13], or extrinsically doped [3]–[5] S/D regions. In this device architecture, the active island is first capped with a double-layer consisting of impermeable SiN_y on permeable SiO_x. The SiN_y layer is subsequently patterned so that it is removed from the channel region. The underlying SiO_x layer, which need not be patterned, acts like an inherent back-channel etch-stop and prevents the channel region from the etch used to define the S/D regions [1]–[16]. The elimination of the patterning step for the etch-stop implies a corresponding reduction in the manufacturing cost of the resulting display panels. During a subsequent heat-treatment in an oxidizing atmosphere, the ρ of the SiN_y-covered S/D regions is significantly reduced. Since the low ρ extends through the thickness of the S/D regions, a reduction in R_p is also anticipated. The channel region, being exposed to the oxidizing atmosphere through the permeable cover, retains its highly resistive character.

The dependence of the hysteresis, the field-effect mobility (μ_{FE}), and the subthreshold slope (SS) of the IGZO TFT with the new architecture on the heat treatment temperature was investigated. All were found to improve with a higher temperature, concurrent with reduction in both the defect population in the channel region and the ρ of the S/D regions.

II. Effects of Thermal Processing on the Resistivity of IGZO

The preparation of the samples started with the room-temperature sputter-deposition of 100-nm IGZO thin film using a target of In_2O_3:Ga_2O_3:ZnO = 2:2:1 mol% in an atmosphere of 10% oxygen (O_2) and 90% argon (Ar). This was followed by the deposition of 100-nm PECVD SiO_x on Sample O and an additional 200-nm-thick PECVD SiN_y on Sample ON. Tetraethylorthosilicate (TEOS) and O_2 were used as the source gases for the former, whereas silane and ammonia were used for the latter. Both depositions were carried out at 300 °C. Sample OT was prepared by replacing the SiN_y of Sample ON with 200-nm titanium sputtered at room-temperature. Uncovered bare IGZO (Sample B) was also prepared. These samples were then subjected to a series of anneals with different annealing temperature, time and ambience, including nitrogen (N_2), O_2, and Ar.

The dependence of the ρ on the annealing atmosphere (Fig. 2) was first investigated by subjecting the samples to 20 min isochronal heat treatments at 450 °C in alternating atmosphere of O_2 or N_2. Prior to measuring the ρ of the covered Samples O and ON using a four-point probe, the cover layers were removed in a reactive-ion etcher (RIE) running a sulfur hexafluoride (SF_6) chemistry. The effects of the etch process on the ρ were minimal, as inferred from the unchanged ρ of a simultaneously etched un-annealed Sample *B*. All samples exhibited n-type conductivity, confirmed using Hall effect measurements.

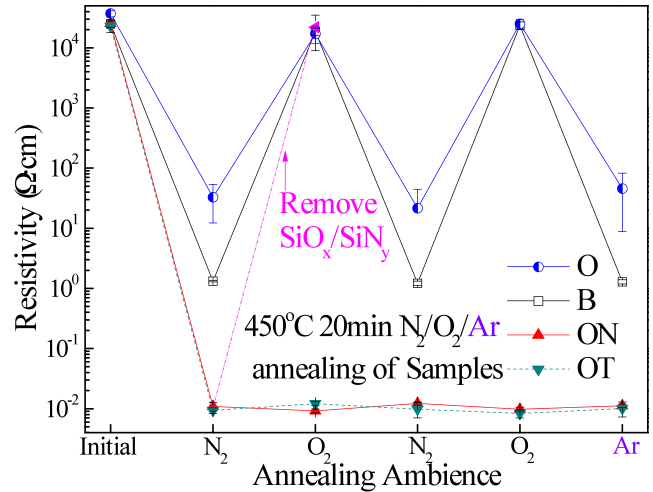

Fig. 2. Dependence of the ρ on the annealing atmosphere (N_2, O_2, and Ar) for Samples B, O, ON, and OT annealed at 450 °C for 20 min.

The ρ of Sample B cyclically changed by over 10^4 times in the alternating atmosphere of N_2 or O_2. The same low ρ was measured on Sample *B* annealed in N_2 and Ar. Since the latter is not a dopant in IGZO, it is unlikely that the charge carriers induced by the annealing in N_2 resulted from doping by nitrogen. Similar dependence of the ρ on the atmosphere was observed for ZnO. This has been attributed to the respective generation and annihilation of intrinsic donor-like defects [12] upon annealing in N_2 or O_2, induced by the exchange of oxygen-carrying species (species for short) between the ZnO and the atmosphere. The generation of donor-like defects in IGZO during N_2 annealing also has been reported previously [7], [8]. Similar dependence of the ρ of Sample O on the cyclical change in the annealing atmosphere was observed, only with a much higher ρ than that measured on Sample B annealed in N_2. This indicates that the oxygen-permeable SiO_x [17] either (1) acted like a diffusion barrier that slowed down the transport or (2) was itself a finite source or sink of the species.

Unlike the ρ of Samples B and O, that of Sample ON was insensitive to the cyclical change in the annealing atmosphere. This behavior, again similar to that observed for ZnO with the same coverage, has been attributed to the top SiN_y cover acting like an impermeable seal [18] that prevented the exchange of oxygen and the species between the ZnO and the atmosphere. The possibility of SiN_y providing hydrogen or nitrogen [4] as potentially extrinsic dopants to IGZO was eliminated using the secondary ion-mass spectrometry. This conclusion was further supported by the similar annealing behaviors of Samples ON and OT (Fig. 2). Furthermore, the ρ of the annealed Sample ON or OT was notably lower than that of Sample B annealed in N_2, hence indicating a difference in either the mechanisms or the rates of the generation of the donor-like defects in the different samples. With the double-layer cover on Sample ON removed after a heat treatment and the resulting sample subjected to a 450 °C 20 min anneal in O_2, the high-ρ IGZO state was recovered.

The dependence of the ρ on the duration of a 450 °C isothermal annealing is shown in Fig. 3. The behavior of

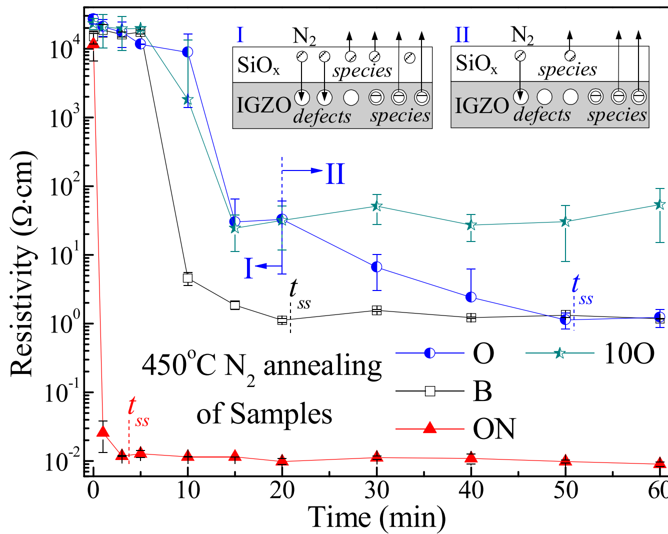

Fig. 3. Dependence of the ρ on the heat treatment time for Samples B, O, ON, and 10O annealed at 450 °C in N_2.

Samples B and ON is characterized by a quick initial drop before reaching a steady-state ρ beyond a corresponding characteristic time (t_{ss}). Both the steady-state ρ and t_{ss} were smaller for Sample ON, indicating more efficient and faster defect generation in the sealed configuration.

A more complicated behavior was observed for Sample O. If the SiO_x cover only retarded the transport of the species, the time evolution of the ρ should be similarly to but have a more stretched-out transition region (i.e., a longer t_{ss}) than that of Sample B. However, an unexpected plateau appeared between an initial rapid drop and a subsequently more gradual decrease for Sample O. In the SiO_x-covered ZnO [12], this behavior has been attributed to the diffusion into the ZnO of the defect-annihilating oxygen-carrying species originating from the SiO_x cover [12]. A plateau appeared when there was a balance between the rates of defect generation and annihilation (Inset I of Fig. 3); and the ρ resumed its gradual reduction when the population of the species in the cover was depleted (Inset II of Fig. 3). Accordingly, a sample with a thicker oxide containing a larger population of species would be expected to have a more extended plateau. This was indeed observed for a sample (Sample 100) covered with a 1-μm-thick SiO_x. Despite the presence of an underlying SiO_x layer, the lack of a plateau for Sample ON could be explained by a sufficiently higher rate of generation of donor defects that overwhelms the supply of the species from the SiO_x layer. This higher rate has already been invoked to explain the lower resistance of Sample ON than that of Sample B, when subjected to the same heat treatment in N_2.

With the annealing temperatures ranging from 400 °C to 700 °C, the time evolution of the ρ was further investigated (Fig. 4). Both the t_{ss} and the steady-state ρ increased with the decreasing temperature for all samples. The consistently high ρ for Sample O annealed at 400 °C suggests a corresponding t_{ss} being longer than 60 min. At a temperature of 500 °C or higher and with a higher defect generation rate overwhelming the species-induced defect annihilation rate, the plateau disappeared and the time-evolution of the ρ of Sample O

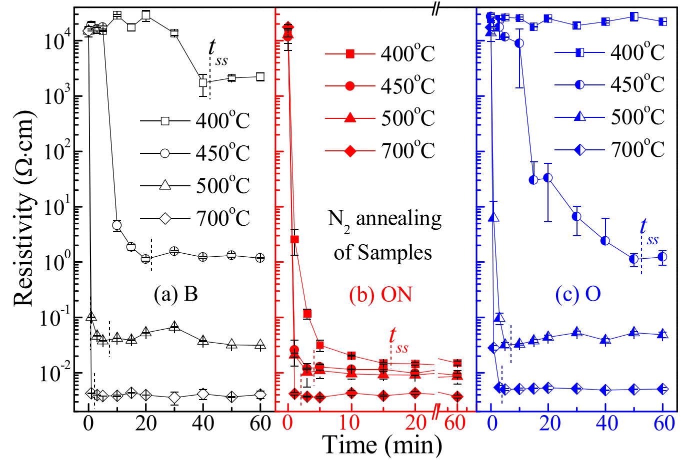

Fig. 4. Dependence of the ρ on the annealing time for Samples B, ON, and O in N_2 at different temperatures.

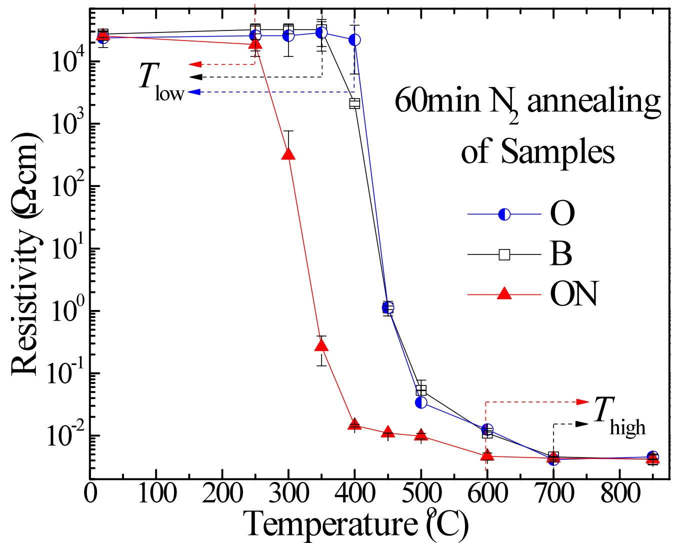

Fig. 5. Temperature dependence of the ρ of Samples B, O, and ON annealed in N_2 for 60 min.

approached that of Sample B. At a given temperature, the configuration ON was consistently the most efficient in turning intrinsic IGZO into a conductor, requiring the shortest t_{ss} and giving rise to the lowest steady-state ρ.

The temperature dependence of the ρ of the samples subjected to 60 min isochronal anneals in N_2 is shown in Fig. 5. The temperature dependence of the ρ revealed a step-like behavior characterized by a low- and a high-transition temperature, denoted, respectively, as T_{low} and T_{high}. The ρ stayed relatively constant and high for an annealing temperature below T_{low} and rapidly dropped to a low and saturated value for an annealing temperature above T_{high}. The saturated values for all three types of samples were similar. These temperatures are different for the different samples, thus making it unlikely that the crystallization of amorphous IGZO is responsible for the observed dependence. This is indeed supported by the X-ray diffraction (XRD) spectra shown in Fig. 6, revealing very little crystallization even after annealing at ~700 °C for 60 min [19].

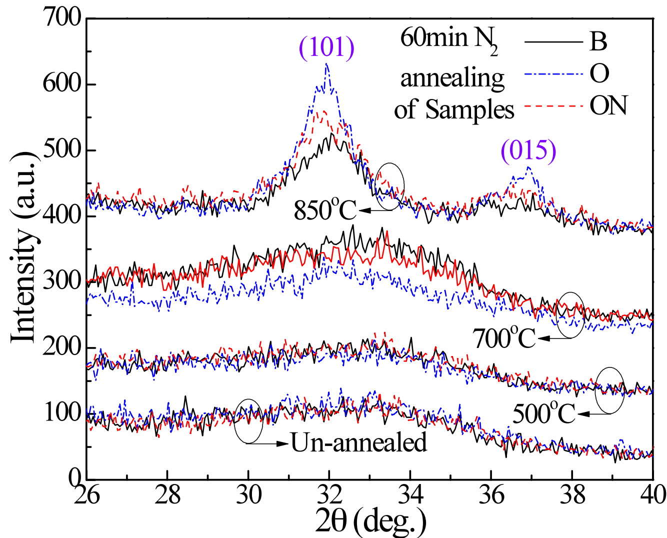

Fig. 6. XRD spectra of Samples B, O, and ON annealed in N_2 for 60 min at different temperatures.

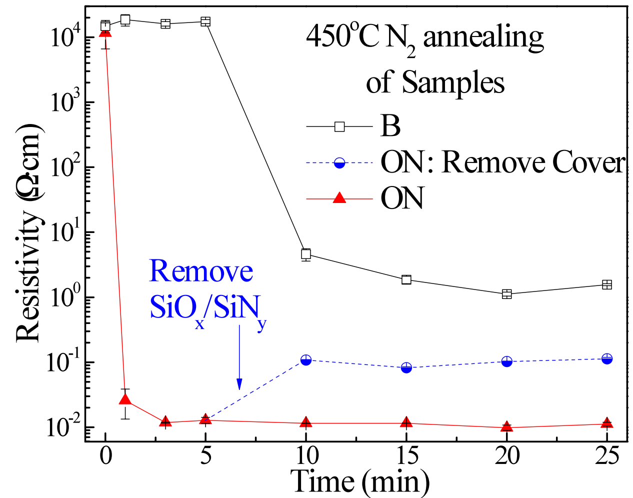

Fig. 7. Dependences of the ρ on the heat treatment time for Samples B, ON with the SiO_x/SiN_x double-layer removed and ON annealed at 450 °C in N_2.

Similar temperature dependence of the ρ of ZnO has been ascribed [12] to the kinetics governing the formation of the donor-like defect. It is plausible that roughly the same is responsible for the trend observed for IGZO. The T_{low} of 450 °C for Sample O, ~50 °C higher than that of Sample B, most likely resulted from the need to exhaust the species originating from the oxide cover of Sample O. The transition temperatures of Sample ON were 100 °C lower than those of Sample B, probably reflecting a lower formation temperature of the donor-like defects in a sealed configuration.

It is possible that the similar annealing behavior reported for both IGZO and ZnO [12] is generally observable in other oxide semiconductors in the same class, albeit with distinctive t_{ss}, transition temperatures, saturation ρ, and mechanisms for different compositions and coverage configurations of metal oxides. This is not to say the behavior of the different oxide semiconductors are entirely the same. An example of a finite difference between the defect-formation mechanisms in IGZO and ZnO is shown in Fig. 7. When the SiO_x/SiN_y double-layer cover on a Sample ON is removed after a heat treatment and the resulting sample is annealed in N_2, the ρ obtained is still roughly 10 times lower than that of Sample B subjected to the same heat treatment. The same is not true for ZnO after similar heat treatment, for which no difference in ρ was observed [12].

III. IGZO TFTs With Annealing-Induced Conductive S/D Regions and Selectively Oxidized Channel

Based on the dependence of the ρ of IGZO on the coverage configuration and the annealing atmosphere, a technology for constructing a TFT without separately deposited [1], [2], [13] or extrinsically doped [3]–[5] S/D regions is demonstrated. The respective coverage configurations of the S/D and the channel regions are made similarly to those of Samples ON and O, thus allowing the use of a single oxidizing heat treatment to form the low-ρ S/D regions, and to simultaneously maintain a device-quality, highly resistive channel region. Compared with previous report [20] on the use of a separately patterned N_2-annealed conductive IGZO (equivalent to Sample B) as the S/D regions, the currently proposed technology is simpler and offers a lower S/D ρ.

Fig. 8 shows the evolution of the schematic cross sections of an IGZO TFT as it is realized using the new process flow. A gate dielectric of 100-nm TEOS SiO_x was first deposited on an n^+ silicon substrate, which would be used as the gate electrode. The room-temperature sputter-deposition of the 100-nm IGZO was followed by the PECVD of 50-nm TEOS SiO_x. After the patterning of the active-island [Fig. 8(a)], a second 50-nm TEOS SiO_x and 200-nm PECVD SiN_y were deposited to form a stacked cover [Fig. 8(b)]. The impermeable SiN_y in the channel region was then removed in an RIE running an SF_6 chemistry [Fig. 8(c)], leaving only the permeable SiO_x covering the channel region. Conventionally, the making of an inverted staggered TFT with a bottom gate [1], [16] resulted in an undesirable but inevitable etching of the back channel. This etching could only be prevented by the formation and patterning of an etch-stop layer [21]. In the present process flow, the SiO_x layer, which does not need to be patterned, serves additionally as an etch-stop and prevents the channel region from being etched. In a subsequent oxidizing heat treatment [Fig. 8(d)], the SiN_y-covered S/D regions were activated and rendered conductive; while the channel region, being exposed to the oxidizing atmosphere through the permeable SiO_x cover, retained its high resistivity. After the S/D contact holes were opened [Fig. 8(e)], the aluminum electrodes were deposited and patterned [Fig. 8(f)]. The resulting TFTs were measured using an Agilent 4156C semiconductor parameter analyzer.

Fig. 9 shows the drain current (I_d) versus gate voltage (V_g) transfer characteristics of TFTs subjected to 10 min isochronal anneals in O_2 at various temperatures. The characteristics were obtained using a cyclic V_g sweep and measured at a drain voltage (V_d) of 5 V. Anticlockwise hysteresis is clearly visible for the TFTs annealed at relatively lower temperatures. Classical linearly extrapolated threshold voltage (V_{th}) is

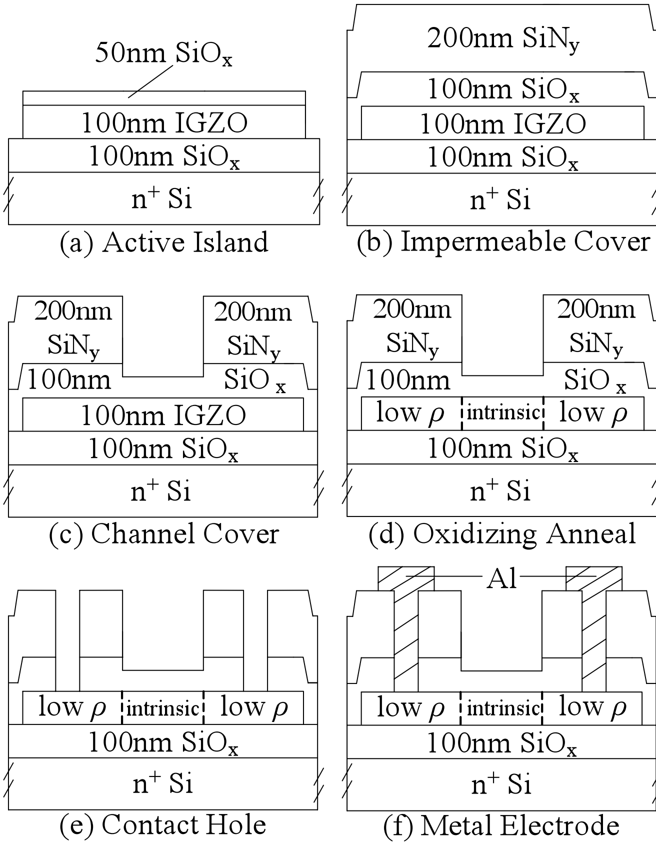

Fig. 8. Schematic of cross sections of an IGZO TFT processed through the proposed technology. (a) Active-island patterning. (b) Formation of the impermeable cover. (c) Channel region patterning. (d) Oxidizing heat treatment. (e) Contact hole opening. (f) Metal electrode patterning.

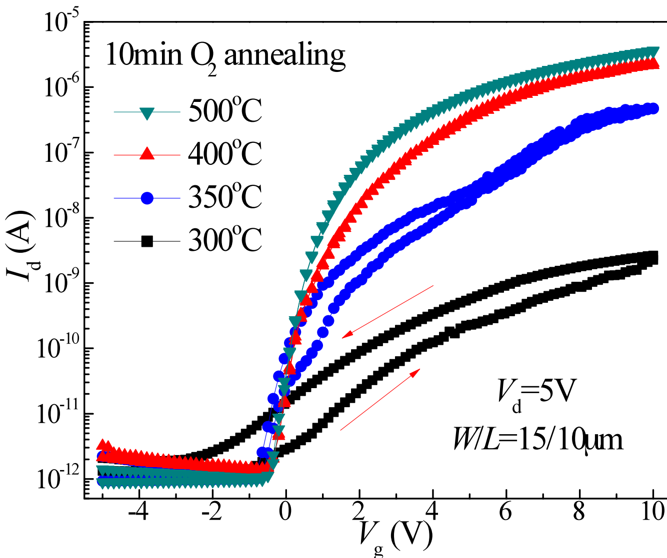

Fig. 9. Transfer characteristics of IGZO TFTs subjected to a series of 10 min isochronal anneals in O_2 at different temperatures.

extracted and its difference (ΔV_{th}) in the two opposite sweep directions is used to quantify the hysteresis. The $|\Delta V_{\text{th}}|$ monotonically decreased with increasing annealing temperature (Fig. 10), becoming unmeasurably small at a temperature near and beyond 400 °C. As in the case of a ZnO TFT [22], the similar suppression of the hysteresis is consistent with

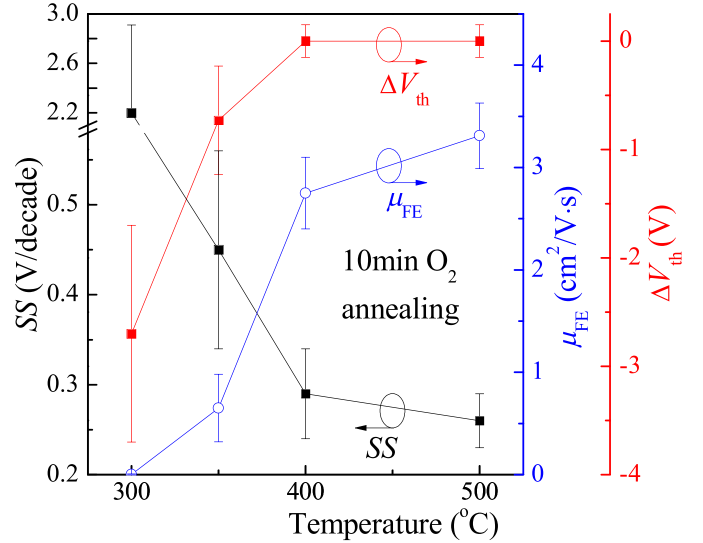

Fig. 10. Temperature dependence of the ΔV_{th}, SS and μ_{FE} for IGZO TFTs annealed in O_2 for 10 min.

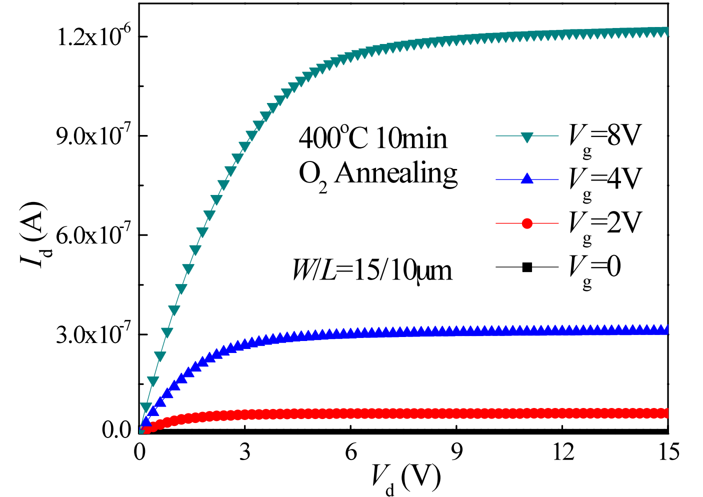

Fig. 11. Output characteristics at various V_g for IGZO TFT annealed in O_2 at 400 °C for 10 min.

the channel-oxidization-induced suppression of the channel defect population and elimination of the H or OH-related dipoles [23], [24] at the interface between the gate dielectric and the channel. Also shown in Fig. 10 are the temperature dependence of the apparent SS and μ_{FE}. Both were extracted without correcting for R_p. The latter was extracted using the maximum $\partial I_d^{0.5}/\partial V_g$ in the saturation regime of the TFT operation. Both parameters continuously improved with increasing annealing temperature and the improvement approached saturation at a temperature near and beyond 400 °C. This temperature dependence is consistent with that of the ρ (Figs. 4 and 5) of Sample ON, reflecting the partial contribution of the reducing S/D ρ (hence also R_p) to the improvement in the two parameters.

The I_d versus V_d output characteristics (Fig. 11) of a TFT annealed at 400 °C exhibit well-behaved linear increase of I_d at low V_d, confirming a good ohmic contact between the metal and the annealing-induced S/D regions. This is consistent with the expectation that the quality of a contact

can be significantly improved by reducing the surface resistivity (Fig. 5) of the S/D regions [3], [25]–[27].

IV. Conclusion

The resistivity of IGZO is found to depend sensitively on both the thermal processing conditions and its cover configuration during the treatment. Based on this observation, a technology for constructing an IGZO TFT with annealing-induced source and drain regions is proposed and demonstrated. The source/drain and channel regions were first capped, respectively, by oxygen-impermeable and permeable covers, thus allowing the channel region to be selectively oxidized while the resistivity of the source and drain regions are being reduced. The permeable cover served additionally as an etch-stop during the patterning of the impermeable cover over the source/drain regions. This prevents the channel region from being exposed to the etch. No additional patterning of such inherent etch-stop is required, thus resulting in reduced manufacturing cost.

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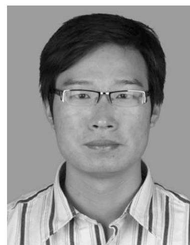

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