Thermally Induced Variation of the Turn-ON Voltage of an Indium–Gallium–Zinc Oxide Thin-Film Transistor

Lei Lu, Jiapeng Li, and Man Wong, *Senior Member, IEEE*

***Abstract*— The thermal processing of an indium–gallium–zinc oxide (IGZO) thin-film transistor (TFT) with annealing-induced source/drain (S/D) regions was found to induce a negative shift in the turn-ON voltage (V_{ON}) of the TFT. Such shifts are consistent with the presence of positive ions, and correlated with the detection of indium, gallium, and zinc, in the dielectric layer adjacent to the channel region. The origin of these species is attributed to the thermally induced dissociation of the IGZO in the S/D regions of the TFT, and the subsequent migration of some of the dissociated species to the dielectric layer above the channel region. It was found that the process-induced shifts in V_{ON} depended on not only the heat-treatment condition but also the structural configuration of the TFT. Since the thermal processes are practically unavoidable during the fabrication of an IGZO TFT and it is unlikely the dissociation of IGZO is unique to the present device architecture, attention must be paid to the effects of the potential migration of such ionic species on the device characteristics, regardless of the transistor structure.**

***Index Terms*— Annealing, dissociation, fixed charge, indium–gallium–zinc oxide (IGZO), permeability, shift, thin-film transistor (TFT), turn-ON voltage.**

I. INTRODUCTION

WITH their relatively low process temperature, high field-effect mobility, low leakage current, and high transparency, indium–gallium–zinc oxide (IGZO) thin-film transistors (TFTs) are being investigated as promising alternatives to low-temperature polycrystalline silicon TFTs for the construction of the next-generation flat-panel displays [1], [2].

Thermal processes are employed during the fabrication of an IGZO TFT for a variety of reasons, such as reducing the source/drain (S/D) and contact resistance, stabilizing the transistor characteristics, and improving the long-term reliability. Yet such processes were also blamed for the generation of donor-defects (such as those attributed to oxygen vacancies) in the channel region of the TFT, thus reducing the channel resistivity (ρ) [3]–[6] and causing a negative shift in the turn-ON voltage (V_{ON}) [3]–[7], where V_{ON} was defined to be the gate voltage (V_g) corresponding to the minimum drain current (I_d) in the I_d versus V_g transfer characteristics of a TFT.

Recently, an IGZO TFT technology with annealing-induced S/D regions was proposed and demonstrated [8]. With a gas-permeable cover placed over the channel region, a high channel ρ could be maintained over a wide range of process temperature when annealed in an oxidizing atmosphere. However, under certain annealing conditions and with certain structural configurations, a negative shift in V_{ON} of the TFT was still observed. Such shift (ΔV_{ON}) is consistent with the presence of positive charges, and correlated with the detection of indium (In), gallium (Ga), and zinc (Zn), in the dielectric layer adjacent to the channel region. The origin of these species is attributed to the thermally induced dissociation of the IGZO in the S/D regions of the TFT, and the subsequent migration of some of the dissociated species to the dielectric layer above the channel region. Since an IGZO TFT is often subjected to various heat treatments during the course of its fabrication and it is improbable that the thermally induced dissociation of IGZO occurs only in the present device architecture, attention must be paid to the potential adverse effects on the device characteristics (such as a finite ΔV_{ON}) of the migration and incorporation of the dissociated ionic species in an dielectric layer adjacent to the channel of the TFT.

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II. TFT FABRICATION AND CHARACTERIZATION

A heavily doped silicon (Si) substrate also serving as the gate electrode was first covered with a 100 nm-thick gate dielectric of silicon oxide (SiO_x) deposited in a plasma-enhanced chemical vapor deposition (PECVD) reactor using tetraethylorthosilicate and oxygen (O_2) as the source gases. A 100-nm-thick IGZO active layer was subsequently sputter-deposited at room temperature using a target of In_2O_3:Ga_2O_3:ZnO = 2:2:1 mol% in an atmosphere of 10% O_2 and 90% argon (Ar). A 50-nm-thick PECVD SiO_x was subsequently deposited before the patterning of the active islands. Following the deposition of the second 50-nm-thick PECVD SiO_x, an additional 200-nm-thick gas-impermeable silicon nitride (SiN_y) was deposited in a different PECVD reactor using silane and ammonia as the source gases [8]. All the PECVD processes were carried out at 300 °C.

SiN_y in the channel region was removed in a reactive-ion etcher running a sulfur hexafluoride chemistry. The underlying

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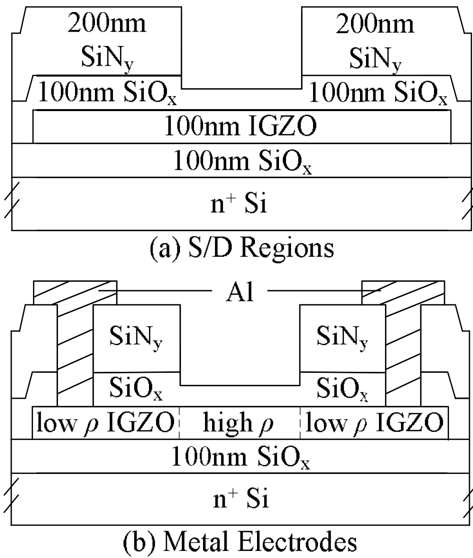

Fig. 1. Schematic cross sections of a bottom-gate IGZO TFT after the patterning of (a) S/D regions and (b) metal electrodes.

SiO_x served as an etch-stop layer and retained as a gas-permeable channel cover [Fig. 1(a)]. During a subsequent annealing in an oxidizing atmosphere at various temperatures and for various durations, the SiN_y-covered S/D regions were activated and rendered conductive, largely due to the thermal generation of donor-like defects [8] rather than the migration of hydrogen from SiN_y [9]. The channel region, being exposed to the oxidizing atmosphere through the permeable SiO_x cover, retained its high ρ. After the contact holes to the S/D regions were opened, the aluminum electrodes were deposited and patterned [Fig. 1(b)]. The characteristics of the resulting TFTs were measured using an Agilent 4156C semiconductor parameter analyzer.

The transfer characteristics, measured at a fixed drain voltage $V_d = 5$ V, of TFTs subjected to 500 °C isothermal annealing for various durations are shown in Fig. 2(a). For heat treatments longer than 20 min, a more negative shift ($\Delta V_{ON} < 0$) in V_{ON} [Fig. 2(a) (inset)] was observed with an increasing annealing time. Such annealing-induced ΔV_{ON} was often [3]–[7] ascribed to higher carrier concentration induced by increased population of donor-defects in the channel region. However, these should normally be accompanied by an increase in the OFF-state current (I_{OFF}) and a degradation in the pseudo subthreshold slope (SS).

In Fig. 2(b), the characteristics were parallel shifted along the V_g axis by the corresponding ΔV_{ON}, and found to largely coincide with that of the TFT annealed for 10 min. The nice overlap of the shifted characteristics, especially the I_{OFF} and SS, reflects a similar residual carrier concentration in the channel region. This is reasonable, since oxygen was allowed to diffuse through the permeable SiO_x to thermally oxidize the channel and to retain its high ρ [8].

Closer inspection reveals a slight increase in and eventual saturation of the ON-state current with longer annealing duration. This is consistent with the increase in and saturation of the apparent field-effect mobility μ_{FE} [Fig. 2(b) (inset)],

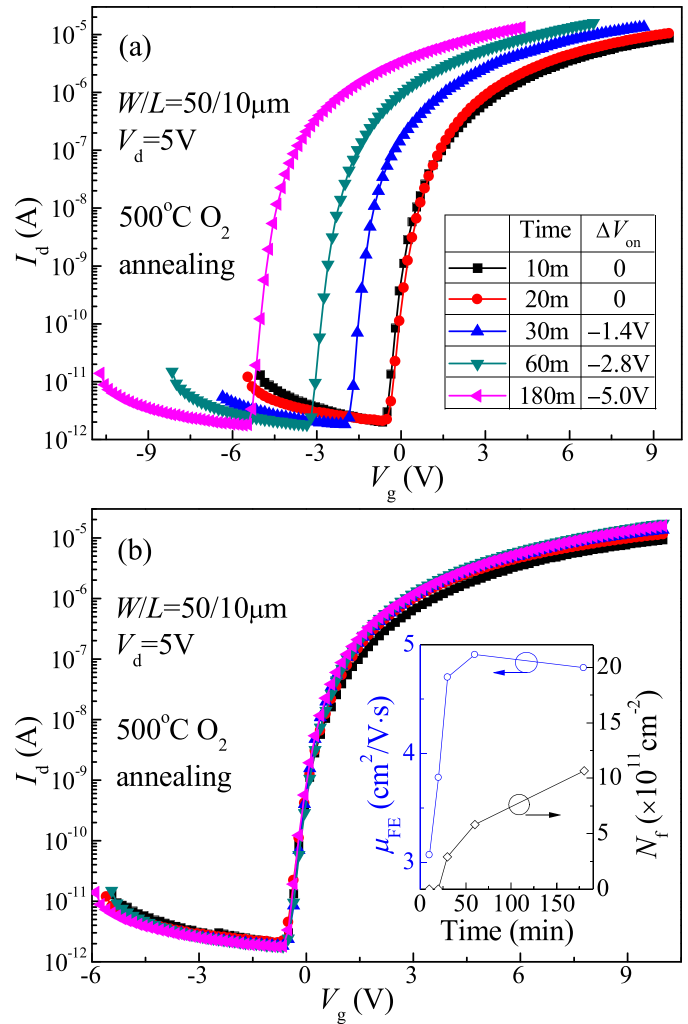

Fig. 2. (a) Transfer characteristics of the IGZO TFTs annealed at 500 °C in O_2 for various durations. Inset: time dependence of ΔV_{ON}. (b) Same characteristics parallel shifted by the corresponding ΔV_{ON}. Inset: time dependence of the estimated N_f and the apparent μ_{FE}.

extracted using the maximum $\partial I_d^{0.5}/\partial V_g$ in the saturation operating regime of the TFT. The effects on μ_{FE} could be attributed to either thermally suppressed defect states in the channel region [10], [11] or a reduced S/D contact resistance due to the annealing-induced reduction of the resistivity of the S/D regions [8].

The observed negative parallel shifts of the transfer characteristics are more consistent with the presence of positive fixed charges (Q_f) in the dielectrics (not merely limited to the gate insulator) adjacent to the channel region. The charge density (N_f) consistent with ΔV_{ON} corresponding to each annealing duration was computed and plotted in Fig. 2(b) (inset).

The temperature dependence of ΔV_{ON} was investigated using a series of 60-min isochronal annealing experiments. The resulting transfer characteristics, again exhibiting an annealing-induced ΔV_{ON} that increased with the higher annealing temperature, are shown in Fig. 3(a). The characteristics are similarly parallel-shifted [Fig. 3(b)] and found to largely coincide with that of the TFT annealed at 400 °C. With ΔV_{ON} assigned again to the presence of

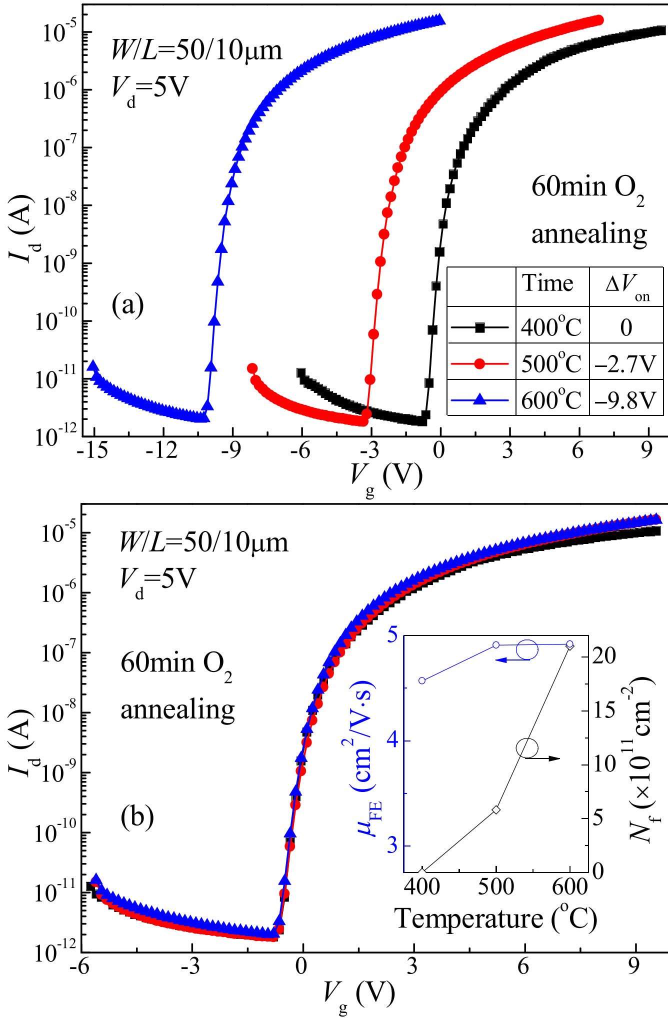

Fig. 3. (a) Transfer characteristics of the IGZO TFTs annealed in O_2 for 60 min at various temperatures. Inset: temperature dependence of ΔV_{ON}. (b) Same characteristics parallel-shifted by the corresponding ΔV_{ON}. Inset: temperature dependence of the estimated N_f and the apparent μ_{FE}.

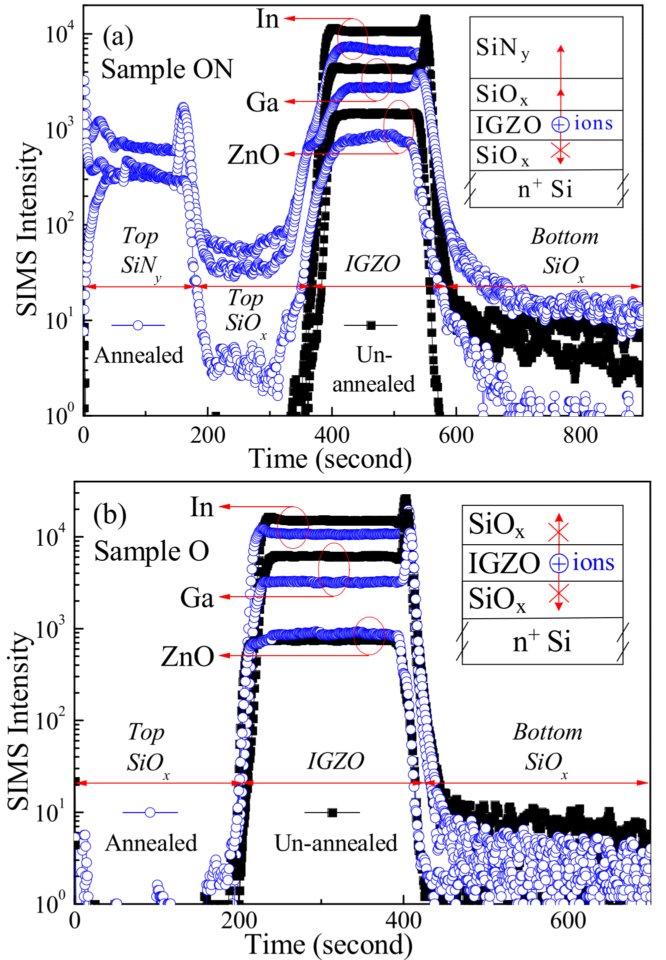

Fig. 4. SIMS profiles of In, Ga, and ZnO in annealed (500 °C in O_2 for 180 min) and unannealed (a) Sample ON and (b) Sample O. Insets: corresponding possible ion-migration paths.

an annealing-induced Q_f, N_f corresponding to each value of ΔV_{ON} is computed and displayed in Fig. 3(b) (inset). The apparent μ_{FE} was also found to slightly increase with the higher annealing temperature [Fig. 3(b) (inset)], again consistent either with the reduced defect states in the channel region or with the reduced S/D contact resistance.

III. Origin of the Dielectric Charge

It can be seen from the schematic cross sections, as shown in Fig. 1, that the annealing-induced Q_f could be located in either the gate SiO_x or the SiO_x cover layer, respectively, below or above the IGZO channel region. Since SiO_x and SiN_y are routinely used in the construction of Si-based transistors, and excessive amount of Q_f has not been observed in the processes involving temperature often exceeding 1000 °C, it is unlikely that Q_f presently observed was spontaneously generated in these dielectric layers, particularly at a low annealing temperature not exceeding 600 °C. A more plausible source of Q_f is the IGZO channel layer, with an abundant supply of In, Ga, and Zn. The presence and distribution of these species in the TFT structure were investigated using secondary ion-mass spectrometry (SIMS).

The preparation of the samples for the SIMS analyses started with the deposition of a 100-nm-IGZO thin film on a SiO_x-covered silicon substrate. This was followed by the deposition of 100-nm-PECVD SiO_x on Sample O and an additional 200-nm-thick PECVD SiN_y on Sample ON [8]. The respective structures of Samples O and ON are structurally similar to those of the channel and S/D regions of the TFT cross sections, as shown in Fig. 1. These samples were subsequently subjected to various annealing schedules.

The distribution of In, Ga, and Zn across the stack of layers in each Sample ON was obtained using SIMS, and shown in Fig. 4(a), where the zinc-oxide (ZnO) complex was used to monitor the Zn content, since the sensitivity of the Zn ion itself is relatively weak. The reference intensities of all the three species were determined using an unannealed Sample ON. It is apparent that the base levels of the intensities in the top SiO_x and SiN_y layers were lower than those in the bottom SiO_x layer, while the changes in the intensities remained small in the bottom SiO_x layer, all the three species increased to abundantly detectable in the top SiO_x and SiN_y layers of Sample ON after having been annealed at 500 °C in O_2 for

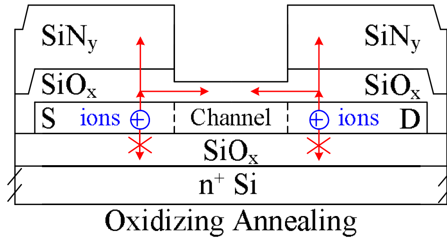

Fig. 5. Schematic of the ion-migration path in a TFT subjected to an oxidizing annealing.

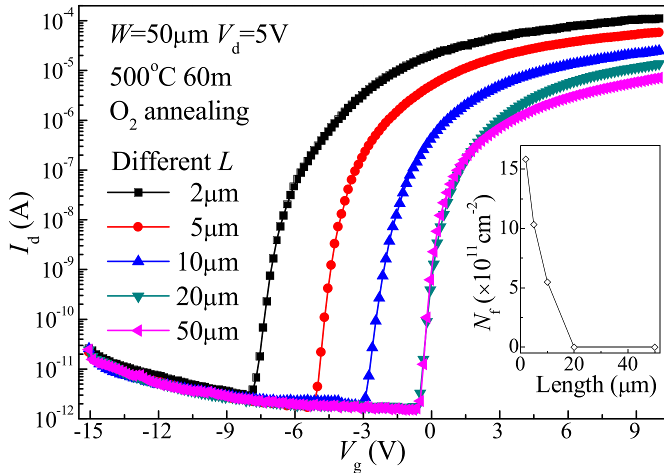

Fig. 6. Transfer characteristics of TFTs with different L's. Inset: L-dependence of the effective annealing-induced N_f.

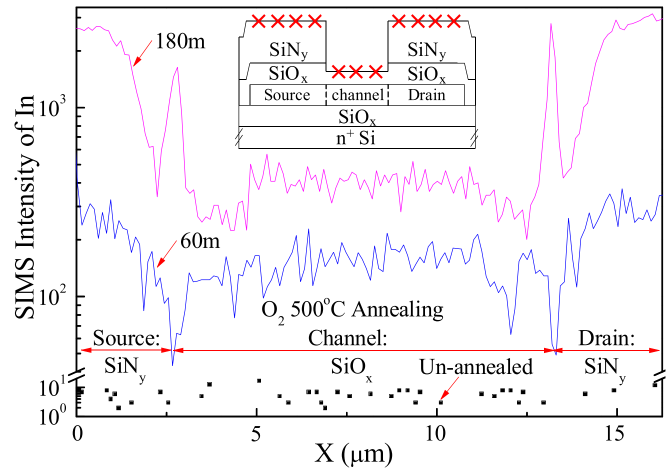

Fig. 7. Distribution of In in the IGZO TFTs annealed at 500 °C in O_2 for various durations. The locations, where the SIMS signal was taken, are indicated by the ×'s in the cross-sectional schematic of the TFT.

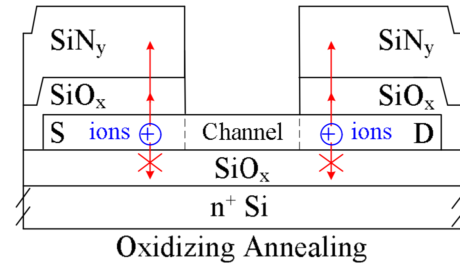

Fig. 8. Schematic of the ion-migration path in a TFT with the elimination of the SiO_x cover layer (hence, also the ion-migration path) over the channel region.

180 min [Fig. 4(a)]. It is presently proposed that these species originated from the thermal decomposition of the IGZO layer, followed by the migration [Fig. 4(a) (inset)] of the dissociated In, Ga, and Zn into the top SiO_x and SiN_y layers.

It is also clear that no significant changes in the depth profiles of the species [Fig. 4(b)] were observed for Sample O after having been subjected to the same annealing schedule. It is believed that the oxidation of the IGZO through the permeable SiO_x cover stabilized the film against decomposition, hence also a lack of the migration [Fig. 4(b) (inset)] of In, Ga, and Zn into the adjacent SiO_x layers.

The absence of the species in the SiO_x layers of an annealed Sample O is inconsistent with the assertion of a Q_f-induced ΔV_{ON} presented in Figs. 2 and 3. It is presently proposed that Q_f responsible for ΔV_{ON} resulted from the lateral diffusion of the ionic species into the SiO_x cover layer in the channel region from the extension of the SiO_x layer in the S/D regions, as shown in Fig. 5. If such lateral diffusion of the species was responsible for the introduction of Q_f into the channel SiO_x cover, one would expect a reduction in the magnitude of ΔV_{ON} with a longer channel length (L) of a TFT. This is indeed observed in Fig. 6.

Direct evidence of the lateral migration of the species, more specifically In, is shown in the scanning SIMS profiles across (Fig. 7) the top surfaces of an unannealed TFT, a TFT annealed at 500 °C in O_2 for 60 min and a TFT similarly annealed for 180 min. The intensities of In increased with the annealing time, particularly in the SiO_x layer above the channel region, from being negligible in an unannealed TFT. The intensities are relatively higher in the SiN_y layers in the S/D regions, consistent with the results shown in Fig. 4(a).

Alternatively, if the SiO_x layer above the channel region was removed during the patterning of the S/D regions, as shown schematically in Fig. 8, one would expect the elimination of the annealing-induced ΔV_{ON}. The transfer characteristics of the TFTs annealed at 500 °C in O_2 for 60 min are shown in Fig. 9. The absence of shifts in V_{ON} is indeed observed, even for a TFT with L down to 2 μm. These results provide further evidence that the decomposed ions did not migrate into the bottom SiO_x layer during annealing. Consequently, it can be concluded that the top SiN_y layer assisted the migration of the species from the decomposed IGZO into the top SiO_x layer; but the same cannot be said of the Si substrate with regard to the bottom SiO_x layer.

IV. Discussion

Metal-oxide TFTs incorporating various permeable (e.g., SiO_x and indium–tin-oxide) and impermeable (e.g., SiN_y, titanium, and some other metals) films [12] as the gate dielectrics, gate electrodes, S/D regions, or passivation layers [1], [2] are inevitably subjected to thermal processes during the course of their fabrication. Indeed, there have been

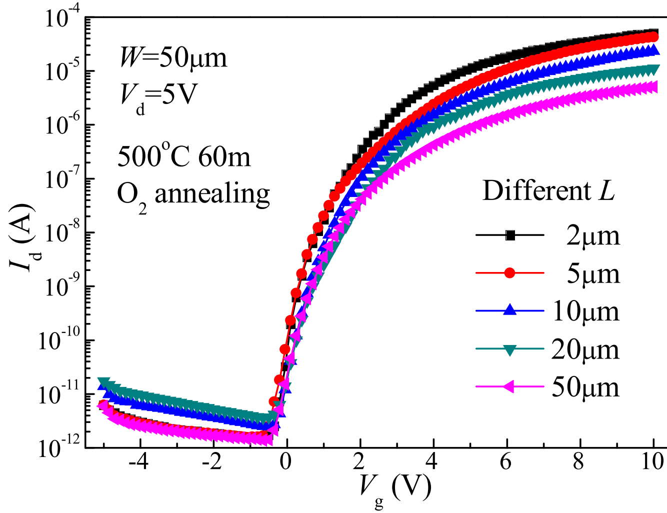

Fig. 9. L-dependence of the transfer characteristics of the IGZO TFTs with uncovered channel regions subjected to 500 °C, 60-min anneal in O_2. Note, the total elimination of the thermally induced ΔV_{ON}.

previous reports on the observation of the annealing-induced ΔV_{ON} in the IGZO TFTs [3]–[7], but attributed to increased concentration of the residual charge carriers resulting from the thermal generation of donor-defects, such as oxygen vacancies [3]–[6], in the channel of a TFT. However, a significant increase in the residual carrier concentration (hence, a reduction in the channel ρ) and defect population should normally be accompanied by an increase in I_{OFF} and a degradation in the SS, particularly for ΔV_{ON} as large as -20 V [7].

The possibility of the impermeable SiN_y acting as a source of hydrogen (H) leading to the doping of the IGZO has been eliminated previously [9], when IGZO with the same low resistance was obtained with SiN_y replaced by titanium (Ti) as an oxygen-impermeable cover layer during the heat treatment. Unlike deposited SiN_y, the intrinsic concentration of H in the sputtered Ti is low. SIMS performed in the S/D and channel regions also revealed a reduction, rather than an increase, in the H concentration in IGZO after the heat treatment (Fig. 10). Finally, SiN_y was similarly present in the S/D regions of a TFT without the SiO_x channel cover (Fig. 8). H, if present in SiN_y, could just as easily diffuse into the channel region from the SiN_y-covered S/D regions. The lack of the V_{ON} shift (Fig. 9) for such a device structure is not consistent with the presence and diffusion of H.

The absence of an increase in I_{OFF} and a degradation in SS, coupled with the structural similarity of the channel region [7] to that of Sample ON, suggests the generation and incorporation of Q_f in the dielectric layer adjacent to the channel as a reasonable alternative explanation for the large ΔV_{ON}. It is unlikely the thermally induced decomposition of common metal-oxide semiconductors, such as IGZO and ZnO, and the subsequent migration of ionic species into the adjacent dielectrics are the phenomena limited to the specific device architecture used in this paper. It is rather a possibility that cannot be ignored for other device structures.

Much remains to be explored and clarified with regard to the mechanism of the migration and the incorporation of

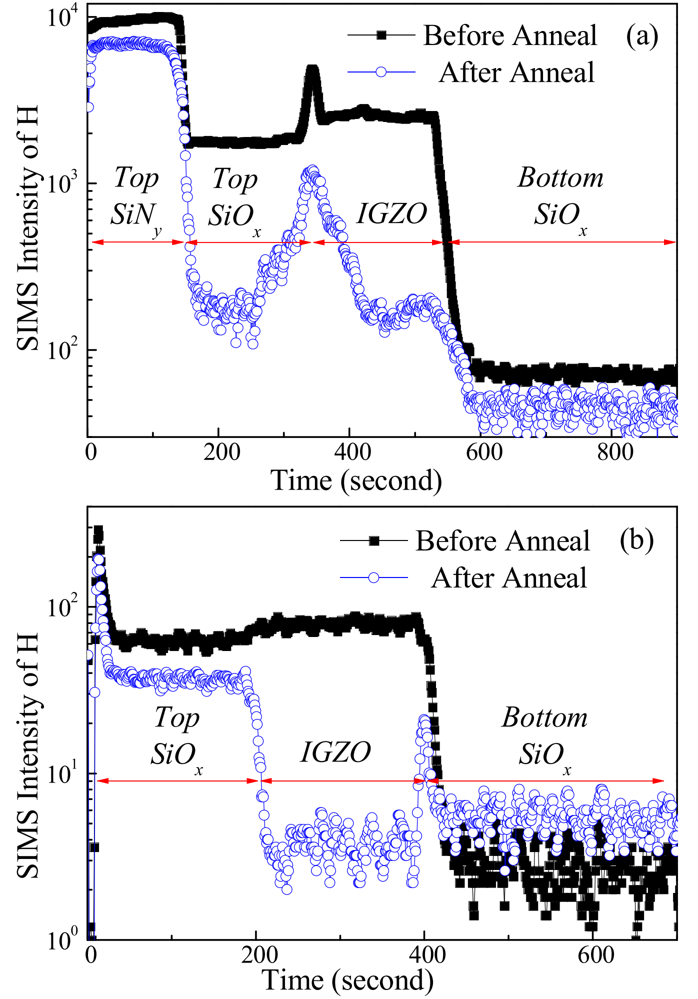

Fig. 10. SIMS profile of H in (a) S/D and (b) channel regions of TFTs before and after being annealed at 500 °C in O_2 for 180 min.

the ionic species in the adjacent dielectric layers. How the SiN_y layer assisted this process in the top but not in the bottom SiO_x layer in the reported device architecture also needs to be investigated. This is a question that is actively being pursued.

V. Conclusion

The thermal processes employed during the fabrication of an IGZO TFT with the annealing-induced S/D regions were found to induce a negative ΔV_{ON}. The change in the device characteristics is attributed to the presence of fixed positive charges in the dielectric layer adjacent to the channel of the TFT. The charges are consistent with the detection of In, Ga, and Zn in such dielectric layer.

The origin of these species is assigned to the thermally induced dissociation of the IGZO in the S/D regions of the TFT, and the subsequent migration of some of the dissociated species to the dielectric layer above the channel layer. It was found that such process-induced ΔV_{ON} depended on not only the heat-treatment condition but also the structural configuration of the TFT. Since the thermal processes are unavoidable during the fabrication of a TFT, general attention must be paid to the possibility of the thermally induced decomposition of the metal-oxide semiconductor, and the subsequent

incorporation of fixed charges in the dielectrics near the channel region of a metal-oxide TFT. A proper process and structure designs must be employed to reduce the sensitivity of the device characteristics to such phenomena.

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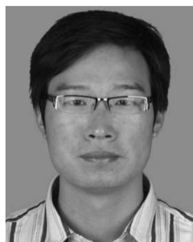

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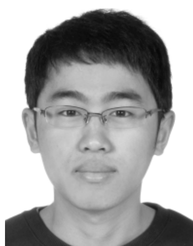

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