Elevated-Metal–Metal-Oxide Thin-Film Transistor: Technology and Characteristics

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***Abstract*— A new device architecture, dubbed elevated-metal–metal-oxide (EMMO) thin-film transistor (TFT), is presently proposed. During a heat-treatment process in oxygen, conductive source and drain regions spontaneously populated by donor defects are formed, while the defects in the channel region are simultaneously passivated. Compared with that of the conventional back-channel-etched TFT, this architecture inherently accommodates an etch-stop/passivation layer without increasing the mask count. EMMO TFT demonstrated using indium–gallium–zinc oxide as an active layer exhibited good performance metrics: a peak field-effect mobility of ∼14 cm^2/Vs, a steepest pseudo-subthreshold slope of ∼120 mV/decade, a leakage current lower than ∼10^{-14} A, an on/off-current ratio above ∼10^{10}, and stability against environmental and electrical stress.**

***Index Terms*— Indium-gallium-zinc oxide (IGZO), thin-film transistor, elevated metal, back-channel etched, mask-count.**

I. Introduction

DUE to their superior attributes, such as transparency, low off-current (I_{off}) and reasonably high field-effect mobility (μ_{FE}), metal-oxide (MO) thin-film transistors (TFTs) are being deployed to replace their silicon counterparts in the backplanes of a new generation of flat-panel displays [1]. Among a range of material candidates, zinc oxide (ZnO) and its variant, indium-gallium-zinc oxide (IGZO) have hitherto been the most commonly studied.

It is generally known that the exposed top-side of the channel of a conventional back-channel-etched (BCE), bottom-gate TFT (Fig. 1a) is damaged [1] during the etching of the source/drain (S/D) electrodes, thus leading to degraded device characteristics. Such damage could be avoided with the incorporation of an etch-stop (ES) layer (Fig. 1b), typically at the expense of an extra patterning step (hence higher manufacturing cost) [2]. It is also possible to avoid the patterning of the ES layer by raising the S/D electrodes to above the passivation layer [3], but this requires an extension of the gate electrode (hence lengthening of the effective channel length) to underlap the S/D contacts. This leads to a larger device foot-print, thus reduced aperture ratio.

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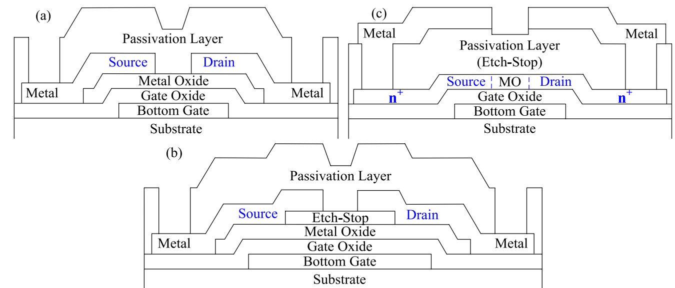

Fig. 1. The schematic cross-sections of (a) a BCE, (b) an ES and (c) an EMMO TFT.

An elevated-metal metal-oxide (EMMO) TFT architecture (Fig. 1b) that retains the simple architecture and the similar foot-print of a BCE TFT is presently proposed. The intrinsic channel region of an EMMO TFT is protected (as in the case of a TFT with an ES layer) during the etching of the elevated electrodes. However, simply elevating the metal electrodes in a BCE structure without lengthening the gate electrode to underlap the contact holes would render inaccessible the field-induced channel. This deficiency is overcome by the incorporation of annealing-induced [4] S/D regions (Fig. 1c).

EMMO TFT constructed using IGZO as an active layer exhibited good performance metrics: a peak μ_{FE} of ∼14 cm^2/Vs; a pseudo-subthreshold slope (*SS*) of ∼120 mV/decade; an I_{off} lower than ∼10^{-14} A; an on/off current ratio above ∼10^{10}; and robust reliability against environmental and electrical stress.

II. Experimental

With an oxidized silicon wafer as the starting substrate, the construction of an EMMO TFT started with the patterning of sputtered indium-tin oxide as the bottom gate electrode. A gate dielectric of 100 nm silicon oxide (SiO_x) was next deposited at 420 °C in a low pressure chemical vapor deposition reactor using silane and oxygen (O_2) as the source gases. In a radio-frequency magnetron sputtering machine with an atmosphere of 10% O_2 and 90% argon at a total pressure of 3 mTorr and a target composition of In_2O_3:Ga_2O_3:ZnO = 1:1:1, an IGZO active layer was deposited at room-temperature. The active island, patterned using a dilute aqueous hydrofluoric acid solution, was then covered with a passivation layer of 300 nm SiO_x deposited using the same process as that for the gate dielectric. The contact holes were next opened in an inductively coupled plasma etcher running a sulfur

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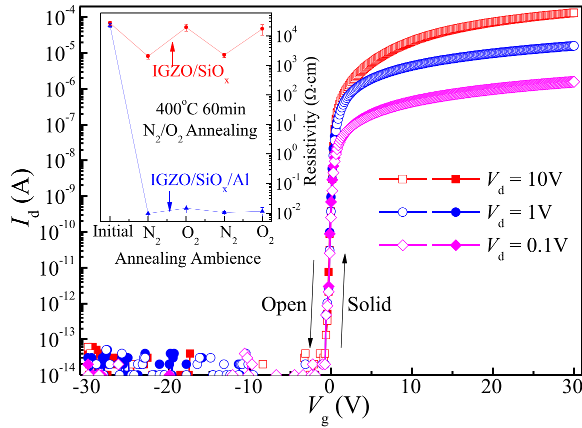

Fig. 2. The transfer characteristics of an EMMO TFT with channel length/width of 42 μm/100 μm. Solid and hollow symbols denote, respectively, forward and reverse V_g sweeps.

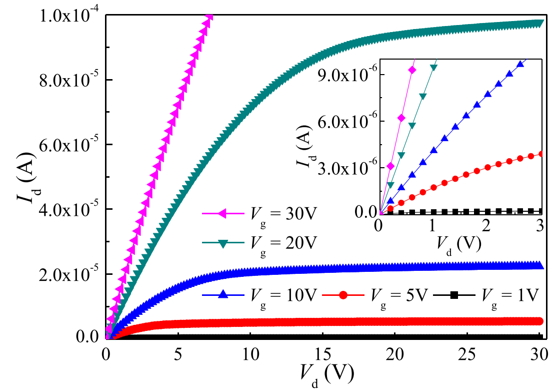

Fig. 3. The output characteristics at various V_g for an EMMO TFT. Shown in the Inset are the output characteristics at low V_d.

hexafluoride chemistry. Finally, with the IGZO intrinsic channel region protected by the SiO_x passivation (thus equivalent to an inherent ES) layer, a sputtered molybdenum/aluminum (Mo/Al) bilayer was patterned to form the S/D electrodes with a 4 μm overlap with the gate electrode.

As shown in the Inset of Figure 2, when IGZO covered with gas-permeable SiO_x was annealed in an atmosphere cyclically switched between nitrogen (N_2) and O_2, a corresponding change in its resistivity (ρ) from low to high was observed. When a gas-impermeable layer of Al was placed on top of the SiO_x, the ρ stayed low regardless of the annealing atmosphere. Similar behavior has been comprehensively reported [4], [5] with silicon nitride as an impermeable cover.

An EMMO TFT is realized by combining gas-impermeable electrodes with a heat-treatment in O_2. Shielded from the oxidizing atmosphere, the active areas covered under the electrodes were converted to annealing-induced conductive S/D regions [4] to access the field-induced channel of the TFT. Exposed to the oxidizing atmosphere through the permeable SiO_x layer, the active channel area not covered by the electrodes remained intrinsic – due to the passivation and suppressed generation [4], [5] of donor-defects.

A series of drain current (I_d) *vs.* gate voltage (V_g) transfer characteristics at different drain voltage (V_d) of an EMMO TFT heat-treated at 400 °C in O_2 for 2 hours were measured using an Agilent 4155C Semiconductor Parameter Analyzer and shown in Figure 2.

A low I_{off} was obtained, below the $\sim 10^{-14}$ A detection limit of the Analyzer. For conventionally processed IGZO TFTs, both the I_{off} and the hysteresis could be degraded by the incorporation during the fabrication process of unintentional external impurities such as hydrogen [6] or the generation of defects such as oxygen vacancies (V_O) [7]. Such process could include the back-channel etch when patterning the metal electrodes [8]; the plasma bombardment when depositing the ES and passivation layers [9] and other improperly designed thermal processes [5], [10]. On the contrary, the oxidizing annealing of the EMMO TFT performed towards the end of its fabrication process – in fact after the formation of the metal electrodes – prevented the formation of donor-defects (thus ensuring a highly intrinsic ρ in the active channel region of the TFT, hence a low I_{off} [10]).

Hysteresis was clearly negligible in the transfer characteristics. This resulted from not only the good quality of the channel region, but also the elimination [11] of residual hydrogen [6], [10], [12]. From the transfer characteristic measured at a V_d of 10V, a steepest *SS* of ~120 mV/decade, a saturation threshold voltage of ~0.4 V extracted from the dependence of $I_d^{0.5}$ on V_g and a peak μ_{FE} of ~14 cm^2/Vs extracted from the maximum $\partial I_d^{0.5}/\partial V_g$ are obtained. The low I_{off}, combined with the reasonably high μ_{FE}, leads to a high on-off current ratio of better than $\sim 10^{10}$.

I_d *vs.* V_d output characteristics (Fig. 3) were also measured at various V_g. The nice linear dependence of I_d on V_d shown in the Inset is a reflection of the good ohmic contact between the highly conductive annealing-induced S/D regions and the Mo/Al metal electrodes.

In addition to the good device characteristics, reliability against environmental and electrical stress has also been studied. Various approaches for reliability enhancement have been proposed: by improving the passivation layer [9], adjusting the composition and oxygen content of the MO [13], modifying the TFT architecture [14], and designing proper process technologies [15], [16]. Shown in Figure 4 is a demonstration of the effectiveness of the 300 nm SiO_x passivation layer against environmental stress. The measured transfer characteristics hardly changed after storage in 90% humidity at 80 °C for 10 hours. The reliability of EMMO TFT against positive/negative bias stress (PBS/NBS) was also investigated, with grounded S/D and respective V_g of +20 and −20 V. The transfer characteristics hardly changed throughout the 30,000 second stress, as is evident from their time evolution in Insets (a) and (b) of Figure 4.

The PBS/NBS-induced degradation in an MO TFT is commonly ascribed to defects in the MO, such as V_O [15], [16]. Suppressing the population of V_O is thus an effective method of enhancing the reliability of a TFT [15]–[17]. One approach is heat-treatment in an oxidizing atmosphere, such as water vapor [15] and air [16]. Consistent with the annealing in an oxidizing atmosphere used in the realization of an EMMO

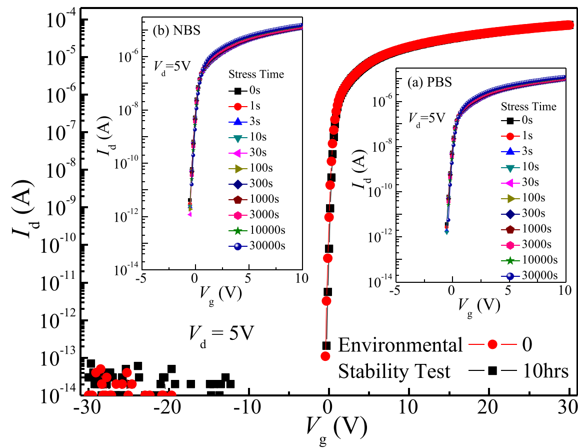

Fig. 4. Comparison of the transfer characteristics of EMMO TFT before and after environmental stress in 90% humidity at 80 °C for 10 hours. Shown in the Insets are the time evolutions of the transfer characteristics of EMMO TFT under (a) PBS and (b) NBS.

TFT, it is not surprising that good reliability against both environmental and electrical stress is obtained.

III. Conclusion

A new bottom-gate metal-oxide transistor architecture, dubbed EMMO TFT, is proposed and demonstrated. The multi-fold superiority of this device structure includes: provision of a spontaneous ES layer without an additional masking step; the ES layer also functioning as a passivation layer against environmental exposure; an oxidation-last annealing heat-treatment ensuring good quality of the intrinsic channel region – thus leading to good device characteristics and reliability.

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