Bottom-Gate Thin-Film Transistors Based on GaN Active Channel Layer

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***Abstract*—GaN thin films were utilized as an active channel layer to produce bottom-gate n-type thin-film transistors (TFTs). The GaN thin films with wurtzite structure were deposited by the reactive dc magnetron sputtering technique using liquid gallium target. The resulting GaN TFTs exhibit good electrical performance, including a field-effect mobility of 5 $cm^2/V \cdot s$, a threshold voltage of 11.5 V, an on/off current ratio of 6×10^6, and a subthreshold swing of 0.4 V/dec. The reported GaN TFTs have great potential in the application of next-generation flat-panel display.**

***Index Terms*—Bottom gate, dc sputtering, GaN, thin-film transistors (TFTs).**

I. Introduction

GALLIUM nitride has emerged as one of the most promising compound semiconductor during the last few years [1]–[4]. GaN-based high-electron mobility transistors are the focus of intense research activities in the area of high-power, high-speed, and high-temperature transistors [1], [2]. The current deposition techniques for high-quality GaN-related thin films are mainly metal–organic chemical vapor deposition (CVD) and molecular beam epitaxy. One of the current directions in GaN research is to deposit high-quality GaN thin films using an inexpensive substrate under low temperature. Recently, amorphous and polycrystalline GaN thin films have been deposited using the magnetron sputtering technique [5]–[8] or the pulsed laser deposition technique [9]. The dc magnetron sputtering technique for the thin-film deposition has the potential of high deposition rate, large area, good uniformity, and low cost suitable for mass production in industry.

Transparent amorphous indium–gallium–zinc oxide (a-IGZO) thin-film transistors (TFTs) have become attractive for use as driving devices in large-scale active-matrix organic light-emitting diode applications, due to their higher mobility and larger area uniformity, as compared with amorphous silicon (a-Si) and polycrystalline silicon (p-Si) TFTs [10], [11]. However, the poor electrical stability of ZnO-based TFTs is still a main issue in preventing commercialization [12]. Bottom-gate and top-gate n-type TFTs using a reactive radio-frequency sputtering GaN thin film as a channel layer have been demonstrated and exhibited poor performance, such as low mobility (6×10^{-2} $cm^2/V \cdot s$) and low on/off current ratio (3×10^3) [13], [14]. We have reported that top-gate n-type GaN TFTs with heavily silicon doped source/drain regions [15] or based on AlN/GaN heterostructures [16] showed good electrical performance. However, they needed high annealing temperature for the activation of the silicon dopant or the formation of source/drain ohmic contacts of the metal alloy.

In this letter, as an alternative to ZnO-based TFTs, bottom-gate n-type GaN TFTs with good electrical performance and low processing temperature were fabricated. The properties of the proposed GaN TFTs were studied and discussed in detail.

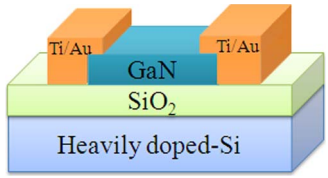

Fig. 1. Cross-sectional schematic of the proposed GaN TFT with a bottom-gate structure.

II. Experiment

The GaN thin films were deposited by reactive dc magnetron sputtering using a liquid gallium target in a mixed Ar and N_2 ambient ($Ar/N_2 = 3{:}14$) at a substrate temperature of 550 °C. The deposition pressure and the input power were 5 mtorr and 80 W, respectively. The structure of the films was analyzed by X-ray diffraction (XRD) experiments in grazing incidence geometry using Cu Kα1 radiation at 40 kV and 40 mA.

The cross-sectional schematic of the proposed bottom-gate GaN TFTs in this letter is shown in Fig. 1. The fabrication process began with a heavily doped n-type crystalline silicon wafer, which was used as the substrate and the gate electrode. A 170-nm-thick low-temperature SiO_2 (LTO) was deposited by low-pressure CVD at 425 °C as the gate insulator. Then, a 150-nm-thick GaN thin film as the active layer was deposited by sputtering on top of the LTO gate insulator at a substrate temperature of 550 °C. The GaN active layer was defined by the photolithography and dry-etching process. The ohmic contacts on source/drain regions were formed by sputtering deposition of Ti/Au (20 nm/50 nm) double metal layers and patterned by the photolithography and liftoff technique, followed by thermal annealing in N_2 ambient at 500 °C for 55 min. The electrical properties of the proposed GaN TFTs were measured at room temperature using an Agilent 4145B semiconductor parameter analyzer.

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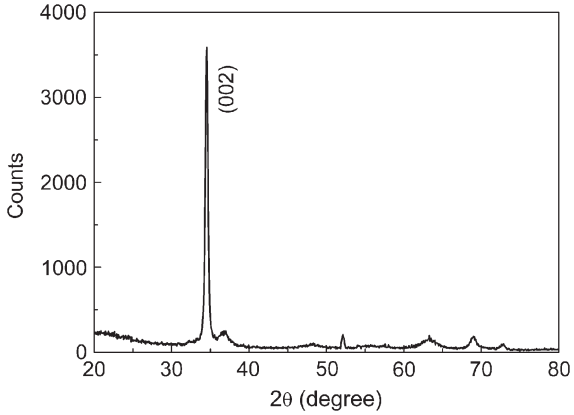

Fig. 2. XRD pattern of the GaN thin film deposited by the reactive dc magnetron sputtering technique.

III. Results and Discussion

Fig. 2 shows the XRD patterns of the GaN thin film deposited at a substrate temperature of 550 °C. Several diffraction peaks were obtained, and the strongest 2θ peak corresponding to (002) was observed at 34.5°, indicating that the GaN film is polycrystalline with a wurtzite structure and has a c-axis orientation. Calculated from the Scherrer formula, the estimated average grain size of the deposited GaN thin film is around 25 nm. The GaN thin films show better crystalline quality with higher deposition temperature, which agrees with the previous report [17].

The field-effect mobility induced by the transconductance at a low drain voltage is given by

$$\mu_{\mathrm{FE}} = \frac{Lg_m}{WC_{\mathrm{OX}}V_{DS}} \tag{1}$$

where g_m and C_{OX} are the transconductance and the gate insulator capacitance per unit area, respectively. The extraction of threshold voltage uses the square root extraction method from the linear relation between ${I_{DS}}^{1/2}$ and V_{GS} in the saturation region. The transfer characteristics with $V_{DS} = 0.2$ V and 5 V for this bottom-gate GaN TFTs are shown in Fig. 3(a). They exhibit good transfer TFT characteristics, such as a linear field-effect mobility of 5 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$, a threshold voltage of 11.5 V, a subthreshold swing of 0.4 V/dec, and an on/off current ratio of 6×10^6. As compared with our previous reports [15], [16], the bottom-gate GaN TFTs studied in this letter show much better performance. One of the reasons for this enhancement of performance may be the better quality of the GaN thin film deposited at a substrate temperature of 550 °C.

The typical output characteristics of the GaN TFTs are shown in Fig. 3(b). The drain–source current I_{DS} exhibits pinchoff and saturation, indicating that the TFTs follow standard field-effect transistor characteristics. The output characteristic shows clear linear regions and does not show significant current crowding at low V_{DS}, indicating that low series resistance R_{SD} in source/drain contacts were obtained.

The R_{SD} was extracted by determining the device on-resistance R_{on} from the linear region of the transfer characteristics and plotting the width-normalized $R_{\mathrm{on}}W$ as a function

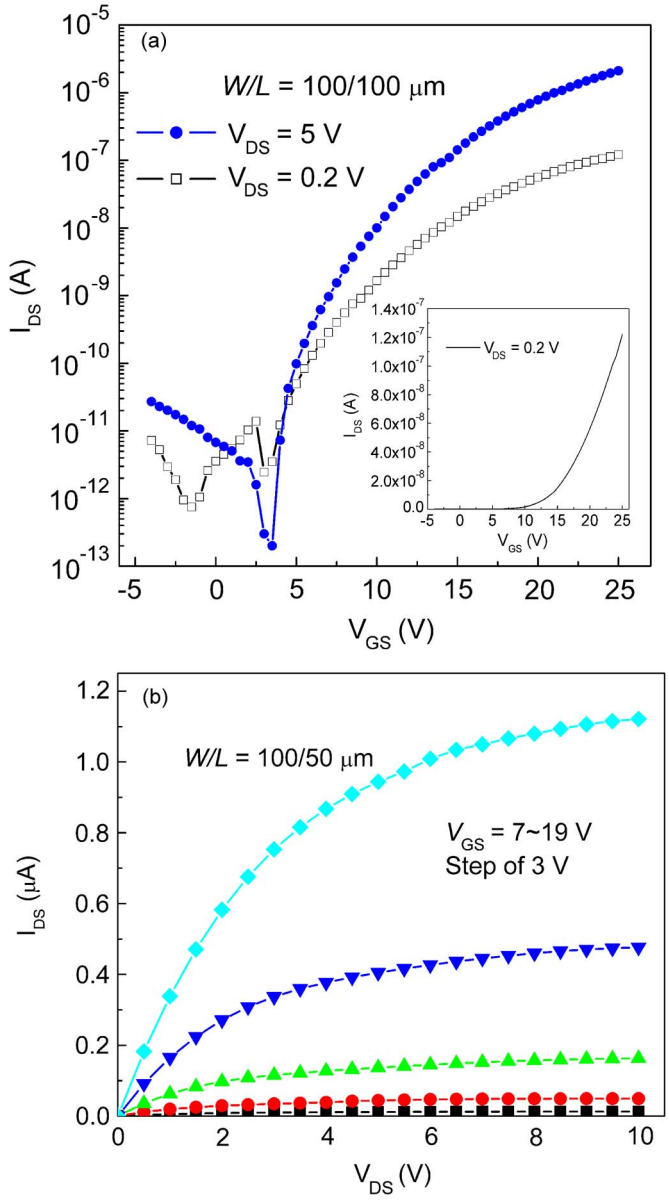

Fig. 3. (a) Transfer and (b) output characteristics of the proposed bottom-gate GaN TFTs.

of the channel length L for different gate voltages. The device on-resistance R_{on} is given in [18], i.e.,

$$R_{\mathrm{on}} = R_{\mathrm{ch}} \times L + R_{SD} \tag{2}$$

where R_{ch} is the effective channel resistance per unit channel length. Fig. 4 shows the width-normalized $R_{\mathrm{on}}W$ as a function of L at different gate voltages at $V_{DS} = 0.2$ V for the GaN TFTs. The $R_{SD}W$ for the GaN TFTs, which is extracted at the y-axis intercept of the extrapolated linear fit of $R_{\mathrm{on}}W$ versus L as given by (2), is approximately 950 $\Omega\cdot$cm, which is similar to that of bottom-the gate a-IGZO TFTs [11]. This low series resistance R_{SD} is caused by the metal alloy Ti/Au deposited by sputtering and thermal annealing process at 500 °C. Different from our previous works with annealing temperature above 850 °C [15], [16], no high temperature annealing is needed for the formation of the source/drain ohmic contacts in this

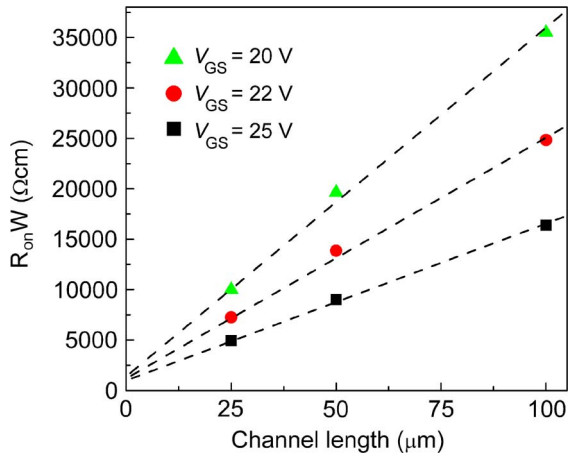

Fig. 4. Width-normalized device on-resistance $R_{\rm on}W$ as a function of channel length L.

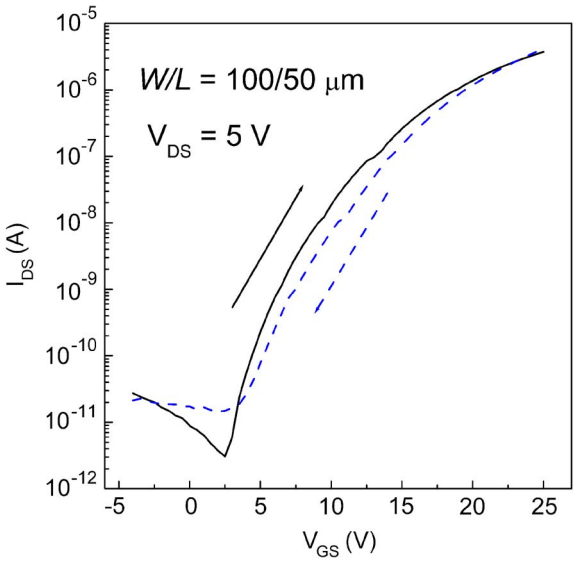

Fig. 5. Hysteresis characteristic of the bottom-gate GaN TFTs.

letter. This low temperature and simple fabrication process are suitable for the application of large-area flat-panel display.

To investigate the effect of SiO_2 gate dielectric and its interface with GaN active layer, the hysteresis of GaN TFT was examined, as shown in Fig. 5. The shift of the threshold voltage for the hysteresis loop was observed. It indicates that some electrons are trapped at or near the interface or within the channel layer, which should be improved in the future.

IV. Conclusion

Good performance bottom-gate n-type TFTs using GaN thin films as active channel layers have been fabricated in this letter. GaN thin films were deposited by the dc reactive magnetron sputtering at a substrate temperature of 550 °C in a mixed Ar and N_2 ambient. Because of the good quality of GaN thin films and the metal alloy Ti/Au for source/drain ohmic contacts, the proposed GaN TFTs have a linear field-effect mobility of 5 $\rm cm^2/V \cdot s$, a threshold voltage of 11.5 V, a subthreshold swing of 0.4 V/dec, and an on/off current ratio of 6×10^6. Due to the low temperature and simple fabrication process, the reported bottom-gate GaN TFTs in this letter can be a potential candidate as driving devices in the next-generation flat-panel displays.

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