High-Performance and Low-Temperature-Compatible Solid Phase Crystallized Polycrystalline Silicon Thin Film Transistors Using Thermal Oxide Buffered Aluminum Oxide as Gate Dielectric

Meng Zhang, Wei Zhou, Rongsheng Chen, Jacob Ho, Man Wong and Hoi-Sing Kwok*

Center for Display Research and Department of Electronic and Computer Engineering
The Hong Kong University of Science and Technology
Clear Water Bay, Kowloon, Hong Kong
(*Email: eekwok@ust.hk)

Keywords: polycrystalline silicon, thin film transistors, thermal silicon oxide, aluminum oxide

ABSTRACT

High-performance and low-temperature-compatible solid phase crystallized polycrystalline silicon thin film transistors using thermal oxide buffered aluminum oxide (Al_2O_3) as gate dielectric are demonstrated. By growing a thermal oxide buffer layer using two-step annealing method, the interface quality is greatly improved, resulting in excellent device performance.

1. INTRODUCTION

Low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) have received great attention in active-matrix liquid crystal displays and active-matrix organic light-emitting diode displays due to their high mobility, which can provide possible solutions for system-on-panel applications [1]. High-performance and low-temperature-compatible polycrystalline silicon (poly-Si) TFTs with small threshold voltage (V_{th}), high driving capability, steep subthreshold swing (*SS*) and low leakage current are thus required to achieve above purpose. Many research works [2-7] on improving LTPS TFTs performance focus on active layer crystalline technology optimization [2-4] and gate dielectric alternation [5-7]. For the active layers, there are three major LTPS technologies, solid phase crystallization (SPC) [2], excimer laser crystallization [3] and metal induced crystallization [4]. Among three methods, SPC is the simplest and the most direct approach to obtain poly-Si film with the high uniformity and low cost [2]. For the gate dielectrics, although scaling down the thickness of SiO_2 could bring higher driving current, the device also suffers from higher leakage current [5-6]. In order to maintain the physical dielectric thickness while increasing the capacitance, several high-*k* materials are used to replace the conventional SiO_2 gate insulator. Among candidate dielectrics, aluminum oxide (Al_2O_3) is a very stable and robust material [7]. It has many favorable properties, such as high band gab (8.7eV), superior reliability characteristic and is amorphous under the conditions of interest [7].

In this work, we studied thermal oxide buffered Al_2O_3 as the gate dielectric for p-channel SPC poly-Si TFTs. The thermal oxide buffer layer was obtained by employing two-step annealing method without increasing process complexity or thermal budget. With this thermal oxide buffered Al_2O_3 as get dielectric, the TFTs exhibit high performance in terms of smaller V_{th}, steeper *SS* and higher on-current (I_{on})/off-current (I_{off}) ratio due to the improved interface between channel and gate dielectric. Both thermal oxide growth and Al_2O_3 film formation are completely low temperature compatible. Furthermore, the device uniformity is also improved by inserting the thermal oxide buffer layer.

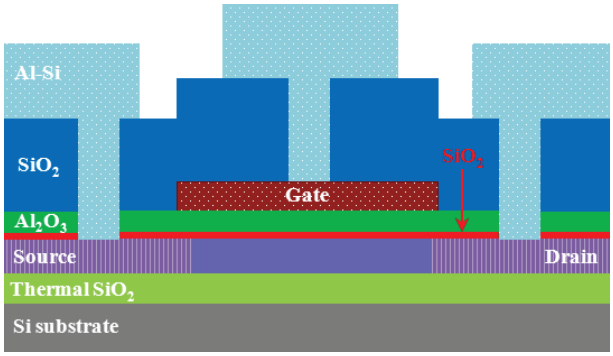

Fig.1: The cross-sectional schematic of poly-Si SPC TFTs using thermal oxide buffered Al_2O_3 as gate dielectric.

2. EXPERIMENTS

The cross-sectional schematic of the self-aligned top-gate p-channel SPC poly-Si TFTs using thermal oxide buffered Al_2O_3 as gate dielectric is shown in Fig.1. First, 500-nm-thick thermal oxide was grown on 4-inch c-Si wafers in furnace. Then, 100nm a-Si active layer was deposited by low-pressure chemical vapor deposition (LPCVD). SPC process was then carried out. In the SPC process, one control wafer was annealed at 600ºC for 24 hours in N_2 ambient while for the other target wafer, it was first annealed at 600ºC for 18 hours in N_2 ambient and then for 6 hours in O_2 ambient. With such two-step SPC treatment, 2.8nm thermal oxide was

obtained on the target wafer with equal thermal budget, compared to the control wafer. After patterning the active islands, 70nm Al_2O_3 was deposited using reactive DC magnetron sputtering method in a mixed Ar and O_2 ambient at room temperature. The deposition pressure and the power were 3mTorr and 120W, respectively. Then 300nm aluminum was sputtered and patterned as gate electrode. Self-aligned 35keV boron implantation was done at a dosage of $4\times10^{15}cm^{-2}$. 500nm LTO was then deposited and contact holes were defined. 700nm Al-1%Si was sputtered. After patterning the metal layer, the devices were sintered in forming gas for 30 min at 420ºC. No further passivation was applied to these devices. For another comparison, devices with 70nm LPCVD SiO_2 as gate dielectric were also fabricated.

For characterizations, atomic force microscope (AFM) and J.A. Woollam M-2000V multi-wavelength ellipsometer are employed to measure the Al_2O_3 film roughness and refractive index (n) respectively. The Agilent 4156B semiconductor parameter analyzer and Agilent 4284A precision LCR meter are used to test the device performance. The V_{th} is determined by the interception of linear extrapolation of a transfer curve at V_{ds}=−0.1V. The SS is also measured at V_{ds}=−0.1V. The I_{on}/I_{off} ratio equals to maximum current over minimum current within the measure range at V_{ds}=−5V. The gate-induced drain leakage (GIDL) current is defined at at V_{ds}=−5V and V_g= 5V. All TFTs used in study have 24μm in width (W) and 10μm in length (L).

3. RESULTS and DISCUSSION

To evaluate the Al_2O_3 film quality, the roughness, relative permittivity (ε_{Al2O3}), breakdown electric field (E_{bd}) and n were measured. Shown in Fig.2 is the AFM image of the 70nm Al_2O_3 film sputtered on bare Si wafer. The root mean square surface roughness is 0.489nm, which is slightly larger than that of atomic layer deposited (ALD) Al_2O_3 film (0.419nm) [6]. The measured capacitance density of Si/53nm-Al_2O_3/Al capacitor with area of 50μm×50μm is about $130nF/cm^2$, as shown in Fig.3. The ε_{Al2O3} of this Al_2O_3 thin film is estimated to be 8.14, which is about two times higher than that of SiO_2 deposited by LPCVD. The E_{bd} calculated from the upper inset of Fig.3 is about 4.1 MV/cm. The leakage current of this capacitor is smaller than 10^{-11}A within the measure range of 5 to −10V (not shown here). The n determined by ellipsometer is shown in the lower inset of Fig.3, which is also comparable to that of ALD Al_2O_3 film [6].

The transfer characteristics of LTPS TFTs with different gate dielectrics were shown in Fig.4. The measured data and the extracted device parameters are summarized in Table I. Apparently, TFT with Al_2O_3 gate dielectric exhibits much better performance than that with conventional deposited SiO_2 except for I_{off}. By applying Al_2O_3 gate dielectric, V_{th} is improved from –13.8V to –4.3V. The SS is also greatly improved, from 1.27 V/dec to 0.60V/dec. However, I_{on}/I_{off} ratio is decreased terribly, from 4.9×10^6 to 2.5×10^4. The thinner equivalent oxide thickness with the same physical thickness of Al_2O_3 dielectrics could explain the lower V_{th} and significantly improved SS [5-7]. By comparing the TFT with Al_2O_3 gate dielectric to the TFT with LTO as gate dielectric, the high I_{off} may be attributed to the large ε_{Al2O3} of Al_2O_3 since the peak electric field near the drain junction is strongly dependent on ε_{Al2O3} [8], which is the key factor to GIDL current [1, 8]. High I_{off} may be also caused by the poor interface between the channel and Al_2O_3. By applying a buffer oxide between the channel and Al_2O_3 as we proposed, both I_{on} and I_{off} are significantly improved, as shown in Fig.4. The I_{on}/I_{off} ratio of LTPS TFT with thermal oxide buffered Al_2O_3 as gate dielectric is increased from 2.5×10^4 to 1.9×10^5.

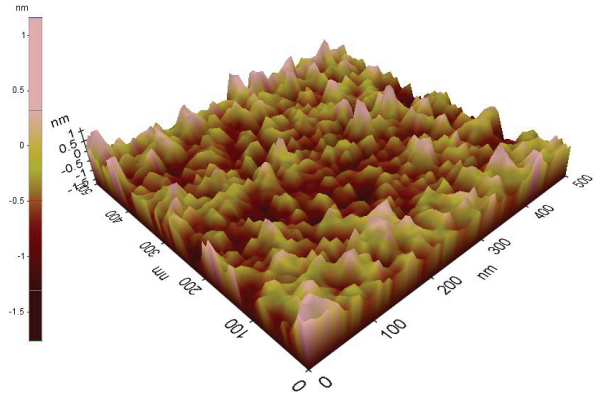

Fig.2: AFM image of the 70nm Al_2O_3 film sputtered on bare Si wafer.

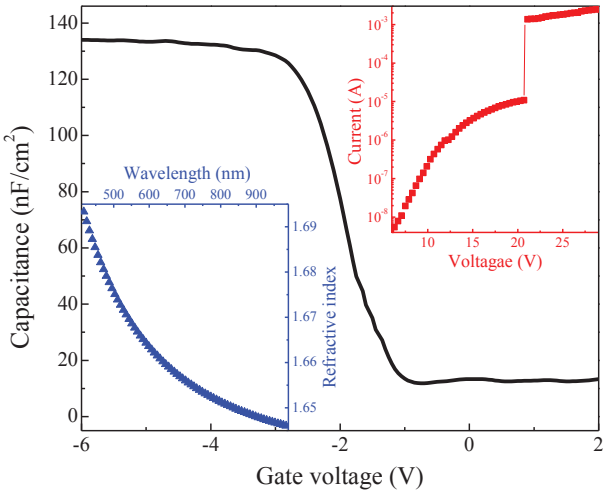

Fig.3: Capacitance density of Si/Al_2O_3/Al capacitor with area of 50μm×50μm, measured at the frequency of 1kHz. The upper inset is the breakdown voltage test and the lower inset the n dependent on wavelength determined by ellipsometer.

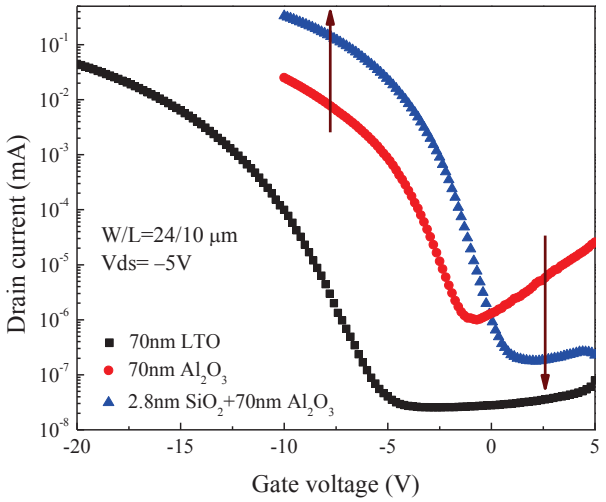

Fig.4: The transfer curves of LTPS TFTs with different gate dielectrics, measured at V_{ds}=−5V.

Table I: Summary of device parameters of LTPS TFTs using different gate dielectrics.

	V_{th} (V)	SS (V/dec)	I_{on}/I_{off}
70nm LTO	−13.8	1.27	4.9×10^{6}
70nm Al_2O_3	−4.3	0.60	2.5×10^{4}
2.8nm SiO_2+70nm Al_2O_3	−3.3	0.59	1.9×10^{6}

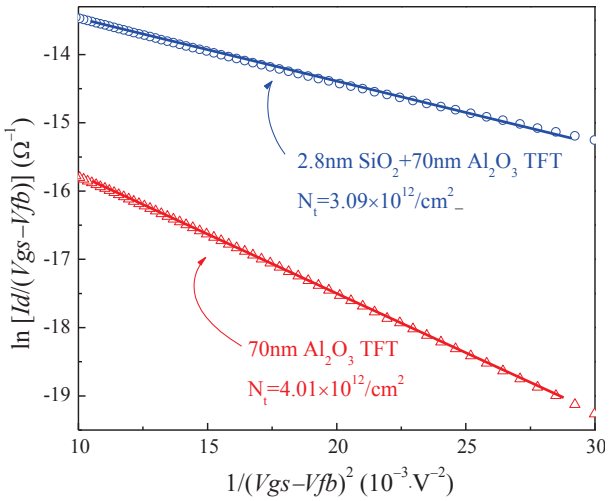

Fig.6: ln[I_d/(V_{gs}–V_{fb})] versus 1/(V_{gs}–V_{fb})^2 curves at V_{ds}=−0.1V for LTPS TFTs using Al_2O_3 gate dielectric with/without buffer thermal oxide.

It is believed that the better performance of LTPS TFT with thermal oxide buffered Al2O3 as gate dielectric is due to the improved interfaces of poly-Si/SiO_2/Al_2O_3. Extracted from transfer curves using the Proano and Levinson method [9-10], the trap state densities (N_t) of LTPS TFT with thermal oxide buffered Al_2O_3 gate dielectric is 3.09×10^{12}/cm^2, which is indeed smaller than that of LTPS TFT with only Al_2O_3 as gate dielectric (4.01×10^{12}/cm^2), as shown in Fig.6.

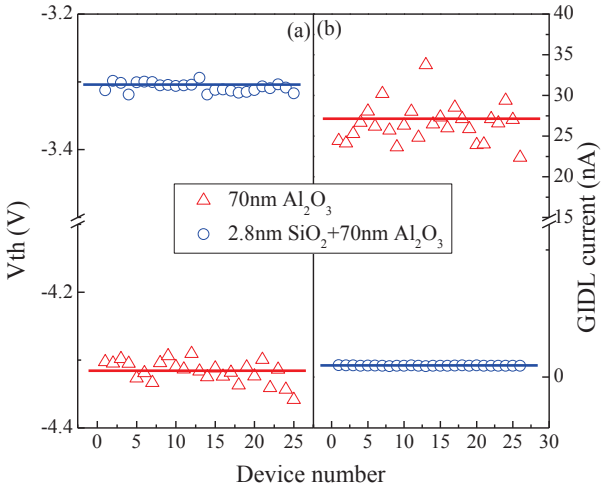

Fig.7: (a) V_{th} and (b) GIDL current variations for 25 TFTs with Al_2O_3 gate dielectric and 25 TFTs with thermal oxide buffered Al_2O_3 gate dielectric.

Besides enhancing the device performance, device uniformity can be also improved by inserting the thermal oxide buffer layer between poly-Si and Al_2O_3. Shown in the Fig.7 are the V_{th} and GIDL current variations for 25 TFTs with Al_2O_3 gate dielectric and 25 TFTs with thermal oxide buffered Al_2O_3 gate dielectric. It can be found that uniformities of both on-state and off-state characteristics are improved by inserting the thermal oxide buffer layer.

4. CONCLUSION

In this work, the low-temperature-compatible SPC poly-Si TFTs using thermal oxide buffered Al_2O_3 as gate dielectric is demonstrated. By inserting the thermal oxide buffer layer between poly-Si and Al_2O_3, the device performance is greatly enhanced due to the better interfaces, especially for improvement of μef and suppression of GIDL current. Furthermore, the device uniformity is also improved by using the buffer thermal oxide layer. Additionally, the buffer thermal oxide layer growth does not increase process complexity at all. Both thermal oxide growth and Al_2O_3 film formation are low-temperature-compatible.

REFERENCES

[1] M. Zhang, M. Wang, H. Wang, and J. Zhou, “Degradation of Metal-Induced Laterally Crystallized n-Type Polycrystalline Silicon Thin-Film Transistors Under Synchronized Voltage Stress,” *IEEE Trans. Electron devices*, 2009, vol. 56, pp. 2726-2732.

[2] N. Yamauchi and R. Reif, “Polycrystalline Silicon Thin-Films Processed with Silicon Ion-Implantation and Subsequent Solid-Phase Crystallization - Theory, Experiments, and Thin-Film-Transistor Applications,” 1994, *J. Appl. Phys.*, vol. 75, pp. 3235-3257.

[3] M. Miyasaka and J. Stoemenos, “Excimer laser

annealing of amorphous and solid phase crystallized silicon films," 1999, *J. Appl. Phys*., vol. 86, pp. 5556-5565.

[4] Z. Meng, M. Wang and M. Wong, "High Performance Low Temperature Metal-Induced Unilaterally Crystallized Polycrystalline Silicon Thin Film Transistors for System-on-Panel Applications," *IEEE Trans. Electron devices*, 2000, vol. 47, pp. 404-409.

[5] M. Yang, C. Chien, Y. Lu, G. Luo, S. Chiu, C. Lou, and T. Huang, "High-Performance and Low-Temperature -Compatible p-Channel Polycrystalline Silicon TFTs Using Hafnium-Silicate Gate Dielectric," *IEEE Electron Device Lett.*, 2007, vol. 28, pp. 902-904.

[6] W. Zhou, S. Zhao, M. Zhang and H. S. Kwok, "Solid Phase Crystallized Polycrystalline Silicon Thin Film Transistors Using Atomic Layer Deposited Aluminum Oxide as Gate Dielectric," *Proceedings of China Display/Asia Display 2011*, pp. 564-567.

[7] G. D. Wilka, R. M. Wallaceb and J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," 2001, *J. Appl. Phys.*, vol. 89, pp. 5243-5274.

[8] M. Hack, I.-W. Wu, T. J. King, and A. G. Lewis, "Analysis of leakage currents in poly-silicon thin film transistors," in *IEDM Tech. Dig.*, 1993, pp. 385-388.

[9] R. E. Proano, R. S. Misage, and D. G. Ast, "Development and electrical properties of undoped polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, 1989, vol. 36, no. 9, pp. 1915-1922.

[10] J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, and M. Rider, "Conductivity behavior in polycrystalline semiconductor thin film transistors," 1982, *J. Appl. Phys.*, vol. 53, pp. 1193-1202.