Study of the Characteristics of Solid Phase Crystallized Bridged-Grain Poly-Si TFTs

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***Abstract*— In this paper, bridged-grain (BG) poly-Si thin-film transistors (TFTs) were fabricated. The characteristics of BG poly-Si TFTs with different BG periods and implantation schemes were investigated. The poly-Si TFTs with optimized BG structures and doping schemes demonstrated greatly improved sub-threshold slope, threshold voltage, maximum field effect mobility, leakage current, and ON/OFF ratio.**

***Index Terms*— Bridged grain (BG), polycrystalline silicon, thin-film transistors (TFTs).**

I. Introduction

LOW-TEMPERATURE polycrystalline silicon (LTPS) technology is one of the most promising candidates to realize high resolution active matrix (AM) flat panel displays. Nowadays, ultrahigh pixel density, which brings strict confinement of the size of the thin-film transistors (TFTs) in the pixel, is required by the smart phone and tablet market. Materials with higher mobility, such as polycrystalline silicon (poly-Si) or metal oxide, which allow smaller transistor size, are therefore taking the place of conventional amorphous-Si (a-Si) as the base material for the TFT arrays. For another emerging trend, that for AM organic light emitting diode (AMOLED) display, poly-Si TFTs are also very competitive due to their higher mobility and good stability.

The most widely adopted LTPS technology is laser annealing. Excimer laser annealing [1] and sequential lateral solidification [2] technology produce poly-Si with fewer defects, but at the same time suffer from material nonuniformity due to the random distribution of grain boundaries [3]. Nonuniformity, which will directly result in nonuniform light emission over the whole panel, is highly undesirable for AMOLED displays. Solid phase crystallization (SPC) technology [4] is well-known to be the simplest and most direct method to convert a-Si into polycrystalline with small but uniform grains. At the same time, the SPC is also known to be the most time consuming method and produces a high density of defects in the crystallized film, which result in poor TFT performance [5]. With the development of magnetic field-aided SPC technology [6], the crystallization process can be greatly accelerated. But, the TFT performance is still not satisfactory for advanced AM applications. Nanostructures have been adopted into TFTs in various ways to improve the device performance. Poly-Si TFTs based on a trenched body [7] have been proposed to control the back-interface conduction in order to reduce the leakage current. Poly-Si TFTs with 3-D finlike channels [8], [9] were also investigated to enhance the gate controllability over the channel geometry and improve the ON-state current, threshold voltage ($V_{\rm th}$), and subthreshold swing (SS). However, the above methods require fine patterning of SiO_2 or poly-Si layers into the nanostructures. Moreover, neither method could significantly improve the ON- and OFF-state characteristics at the same time.

Bridged-grain (BG) technology [10] has been introduced to improve the ON/OFF-current ratio, $V_{\rm th}$, SS, and gate-induced drain leakage (GIDL). The benefits of employing a BG structure originate from several aspects. First, in the ON-state, the short channel effects are beneficially employed to reduce the $V_{\rm th}$ and increase the carrier mobility. Second, the grain size effect: when the grain size is made comparable with the channel length, the BG regions provide shortcuts to the carriers, and help the carriers to and the more conductive path. The number of barriers and traps along the current path is greatly reduced, which would directly result in lower $V_{\rm th}$, sharper SS, and higher mobility. Third, in the OFF-state, the detrimental effect of a higher leakage current associated with the short channel effects is overcome by the multijunction effects [11] that are inherent in the BG structure due to the reduced electric field near the drain.

For the grain size effect, minimizing the number of grain in the channel can be realized through reducing the length of each subchannel and adopting poly-Si material with larger grain size. For the multijunction effect, adopting larger number of subchannels helps lowering the drain electric field more efficiently. When the channel length on the layout is fixed, using shorter subchannels is a way to enhance the above-mentioned effects. However, as the subchannel length getting scaled, the detrimental aspects of short channel effects exhibited. In short-channel TFTs, the $V_{\rm th}$ in the linear region decreases due to the reduction of charge in the depletion layer. In the

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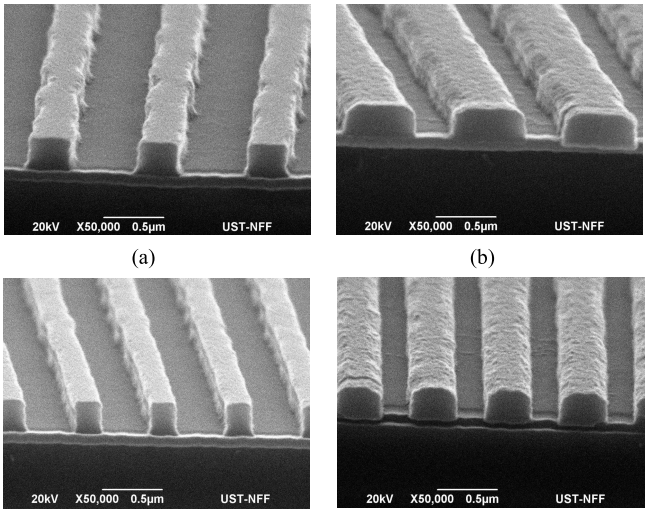

Fig. 1. SEM images of the patterned photoresist gratings. (a) Positive photoresist $\Lambda = 800$ nm. (b) Negative photoresist $\Lambda = 800$ nm. (c) Positive photoresist $\Lambda = 600$ nm. (d) Negative photoresist $\Lambda = 600$ nm.

saturation region, drain-induced barrier lowering effect causes an injection of extra carriers and result in larger ON-state current and lower V_{th}. Under high drain bias, punchthrough effect occurs and carriers in the source region can be injected into the depletion region and swept by the field and finally collected at the drain. When punchthrough happens, the SS become worse, leakage current increases. Under significant punchthrough, the gate will lose control over the drain current.

To prevent punchthrough and maximize the BG effect, the BG configuration and doping scheme must be optimized. In this paper, we investigated the device characteristics of the BG TFTs with different BG periods and doping schemes to study the effect of various process parameters on the performance of the BG TFTs. Although laser interference photolithography is applied in this paper to make the grating layer with the period smaller than 1 μm as the mask for the BG doping, it should be noted that this grating layer could also be conveniently fabricated over a large area at low cost by adopting nanoimprint technology [12].

II. Device Fabrication

Four-inch sized silicon wafers covered with 500-nm thermal oxide were applied as the starting substrates and 100-nm a-Si was deposited from silane (SiH_4) onto the substrate through low-pressure chemical vapor deposition (LPCVD) at 550 °C as the active layer. The SPC process was then carried out through annealing at 600 °C for 24 h in N_2 to convert the a-Si layer into poly-Si. After crystallization, antireflection coatings (ARC) and photoresist were spin coated. The photoresist layer was then patterned into gratings with different periods (Λ) and aspect ratios. Structures of the patterned photoresist were captured by the scanning electron microscope (SEM) and are shown in Fig. 1.

Boron ions were then implanted into the exposed areas through the grating at a dose of $2 \times 10^{15}/\text{cm}^2$. To investigate the effect of different implantation schemes, the implantation

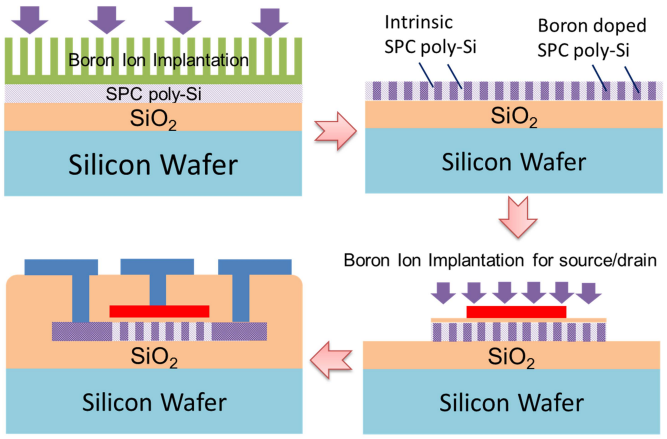

Fig. 2. Key steps of the process flow of BG-SPC TFT fabrication.

TABLE I
Summary of Process Parameters of BG-SPC TFTs

Sample Name	*Period (nm)*	*Aspect Ratio (Exposed: Covered)*	*Implantation Energy(keV)*
600-13	600	2:1	13
600-23	600	2:1	23
600-23N	600	1:2	23
800-13	800	2:1	13
800-23	800	2:1	23
800-23N	800	1:2	23
SPC	No BG	N.A.	N.A

energy was varied. After implantation, the photoresist and ARC layer were removed and the poly-Si layer was then patterned into active islands, followed by 70-nm SiO_2 deposition through LPCVD at 425 °C as gate dielectric. Then, 200-nm titanium was sputtered and patterned as gate electrodes and the source and drain were formed through a self-aligned 33-keV boron implantation at a dosage of $4 \times 10^{15}/\text{cm}^2$. The contact holes were defined through another 500-nm SiO_2 layer, which was adopted as an isolation layer. A 700-nm Al-1%Si was sputtered and patterned as testing pads. The devices were then sintered in forming gas for 30 min at 420 °C. No further passivation was applied to these devices. The schematic view of the fabrication process of the BG SPC TFT is shown in Fig. 2.

Table I is given here to summarize the BG periods, exposure fractions, and implantation schemes used in the BG TFTs.

The samples were named in the format of BG period-implantation energy, and the letter N was added if the BG lines were formed using a negative photoresist. For example, 600-23N represents the BG-TFT with a 600-nm period and negative photoresist patterned BG lines, and the implantation energy used was 23 keV.

III. Results and Discussion

Measurements of device characteristics were done using an HP4156B semiconductor parameter analyzer. The channel width (W) to length (L) ratio of the TFT is 24/10 μm on the layout. The key parameters of the six types of devices together with the reference SPC TFT without BG are summarized

TABLE II
SUMMARY OF DEVICE PARAMETERS OF BG-SPC TFTS

Sample	600-13	600-23	600-23N	800-13	800-23	800-23N	SPC
L(μm)	10	10	10	10	10	10	10
L_{eff}(μm)	3.33	3.33	6.67	3.33	3.33	6.67	10
V_{th}(V)	-8	-4.5	-10.4	-11.5	-9.4	-117	-13.8
SS(V/dec)	1.15	N.A.	1.06	1.17	1.1	1.17	1.72
on-off ratio ($\times 10^6$)	15.2	N.A.	76.8	35	53.1	53.9	1.34
G_m(nS)	955	1141	616	785	1020	558	229
μ_{FE} (cm^2/Vs)	26.1	N.A.	33.9	21.5	28.1	30.7	19.3
GIDL (pA/μm)	29.4	N.A.	1.89	124.5	1.43	2.58	613

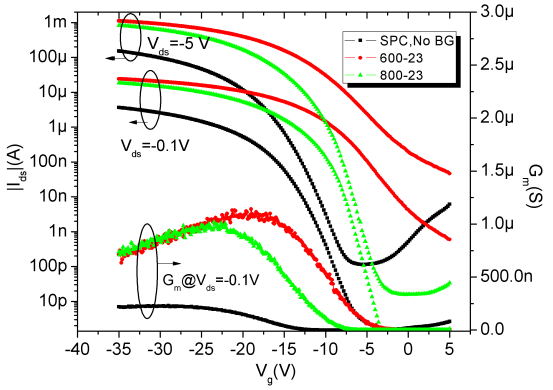

Fig. 3. Transfer characteristics of BG-SPC TFTs with different BG periods.

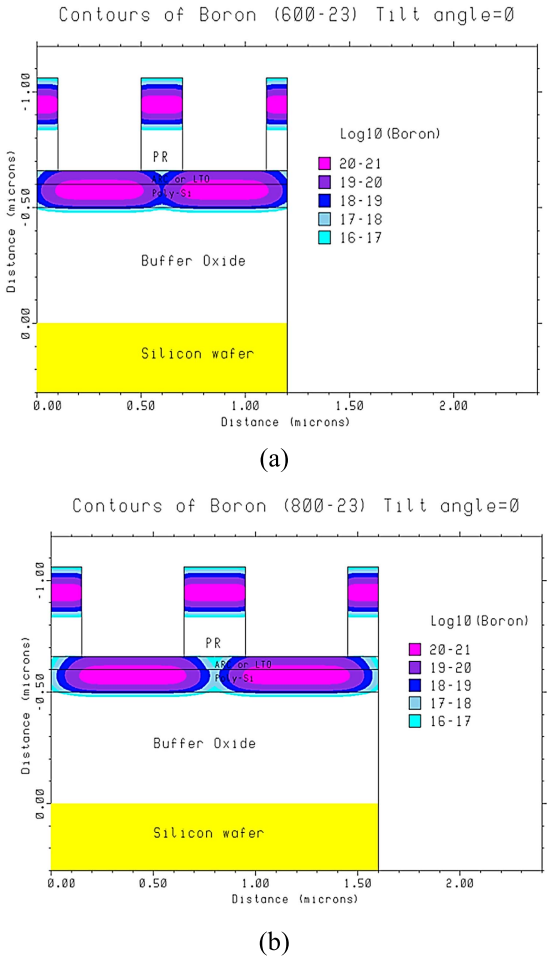

Fig. 4. Contour plots of dopant distribution for samples with different period of BG lines. (a) 600-23. (b) 800-23.

in Table II. The effect of different BG periods, implantation energy, and aspect ratio are investigated, respectively. Here, the $V_{\rm th}$ is defined as V_g when $|I_d|$ reached W/L $\times 10^{-7}$ A at $V_d = -5$ V. The ON/OFF current ratio is defined as the ratio of maximum and minimum value of $|I_d|$ at $V_{\rm d} = -5$ V. G_m stands for the maximum value of transconductance at $V_d = -0.1$ V. The effective L ($L_{\rm eff}$, equals 1/3 or 2/3 of the L on the layout, depending on the aspect ratio of the grating) is used in the calculation of $\mu_{\rm FE}$. The field effective mobility ($\mu_{\rm FE}$) is estimated using the equation: $\mu_{\rm FE} = L_{\rm eff} G_m / W C_{\rm ox} V_{\rm ds}$, where $C_{\rm ox} = 4.93 \times 10^{-4}$ F·m^{-2}.

A. Effect of Changing BG Periods

For the samples 600-23 and 800-23, the conditions for the BG ion implantation are 23 keV, 2×10^{15}/cm^2. From the SEM images of the grating shown in Fig. 1 and the parameters listed in Table I, it is recognized that the effective channel lengths for these samples are almost the same (i.e., 1/3 of the original channel length). The only difference is the period of the BG lines. The effect of the BG period on the device performance is studied through these two samples. The transfer characteristics of BG-TFT 600-23, 800-23 and the reference SPC TFT without BG measured at $V_{\rm ds} = -0.1$ V and -5 V are shown in Fig. 3. From Fig. 3, it can be seen that the BG-TFT (sample 800-23) exhibits great reduction in $V_{\rm th}$, ON/OFF current ratio, G_m, and SS. These advantages of the BG have been attributed to the grain size effect and short-channel effect for the enhanced $V_{\rm th}$, ON-state current and SS, and the drain electric field reduction for the leakage current control. For sample 600-23, although larger ON-state current and G_m are observed as we predicted, the OFF-state current is even larger than that of the reference SPC TFT without BG. The poor OFF-state performance of sample 600-23 is due to the lateral scattering of dopants during the BG implantation process.

In an ion implantation process, the collision of the dopant and host is a statistical process. Therefore, for certain implantation energy, the dopant distribution in the host roughly follows a Gaussian function along the depth of the material. The off-axis scattering also results in the lateral expansion of the dopant distribution profile. The projection range and straggle can be simulated using semiconductor process simulation software such as TSUPREM-4. The simulation results are shown in the contour plots shown in Fig. 4(a) and (b) for the two cases discussed above.

It can be seen that for sample 600-23, the small period and lateral scattering result in a wide spread of dopants into the

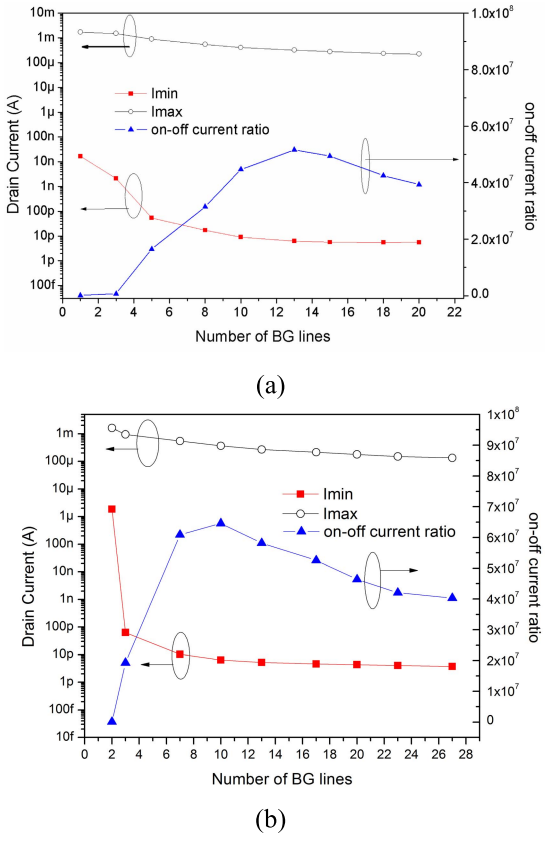

Fig. 5. Plot of I_{max}, I_{min}, and ON/OFF current ratio versus number of BG lines. (a) Sample 800-23. (b) Sample 600-23N.

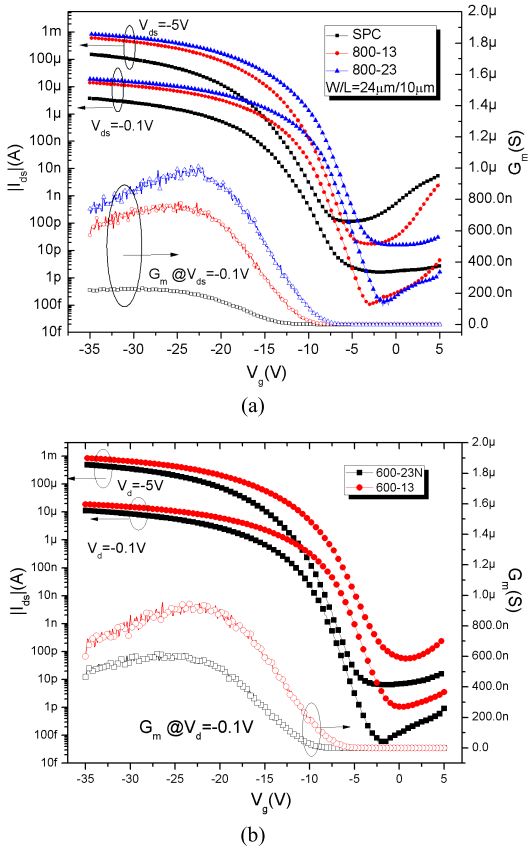

Fig. 6. Transfer characteristics of BG-SPC TFTs with different implantation energies. (a) 800-13 and 800-23. (b) 600-13 and 600-23N.

regions protected by the photoresist. The doping concentration in the channel is above $1 \times 10^{18}/\text{cm}^2$, which makes the short channels start to be conductive. As a result, although the ON-state current for sample 600-23 is larger, the TFT cannot be turned OFF. For sample 800-23, the channel dopant concentration is more than one order lower than 600-23. From Fig. 3, it can be seen that sample 800-23 works properly, with obvious improvement of device characteristics compared with the device without BG.

For sample 800-23 and 600-23N, the relationship between the number of BG lines and the maximum/minimum drain current (I_{max} and I_{min}, respectively) and ON/OFF current ratio are plotted in Fig. 5(a) and (b), respectively. The channel length on the layout is varied from 1 to 16 μm, resulting in 1–20 BG regions in the channel for 800-23, or 2–27 BG regions for 600-23N. The width of the channel is fixed to be equal to 10 μm.

Fig. 5 shows that I_{max} decreases for both samples with a larger number of BG lines, which is due to the longer effective channel length. Sample 800-23 shows a larger ON-state current due to shorter effective channel length. I_{min} also decreases with a larger number of BG lines, but the decrease of I_{min} is not only due to the channel length variation, but is also due to the drain electric field lowering effect. Therefore, the ON/OFF ratio is not simply a constant for different channel lengths, as shown in the blue curve in Fig. 5(a) and (b). The effect of the drain electric field lowering is saturated when the number of BG lines is large enough. Further increasing the number of BG lines shows no benefit to the ON/OFF current ratio due to the reduced ON-state current. The ON/OFF ratio already reaches 1×10^7 when there are five lines (i.e., 4-μm channel length) in the channel for 800-23, and it reaches a maximum value of above 5×10^7 when there are 13 lines (i.e., 10-μm channel length). Saturation of current ON/OFF current ratio happens at a smaller BG number for sample 600-23N, due to the longer subchannel length (~400 nm for each subchannel) and less short channel effect than in sample 800-23. With 6-μm channel length on the layout (10 BG lines in the channel), the ON/OFF ratio can be as high as 6×10^7. Therefore, when the channel length is fixed, it is preferred to have a shorter BG period in order to introduce more BG lines in the channel. However, the separation between neighboring short channels must be properly chosen, with careful consideration of the lateral distribution of dopants, as discussed above.

B. Effect of Changing Ion Implantation Energy

For the samples 800-13 and 800-23, the conditions for the BG ion implantation energy are 13 and 23 keV, respectively, with the same dose of $2 \times 10^{15}/\text{cm}^2$. The number of BG lines in the channel and the effective channel lengths are the same. The transfer characteristics of BG-TFT 800-13, 800-23 and the reference SPC TFT measured at $V_{ds} = -0.1$ and -5 V are shown in Fig. 6(a).

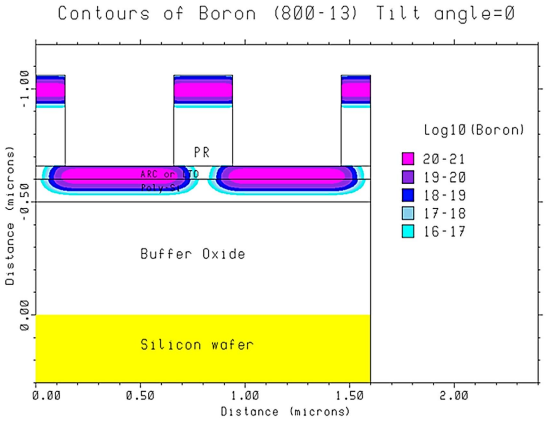

Fig. 7. Contour plots of dopant distribution for sample 800-13.

It can be observed that 800-13 shows much less reduction in V_{th} and GIDL than 800-23. However, the SS, maximum ON-state current and minimum leakage current of these two samples are comparable. The boron dopant distribution profiles are simulated and shown in Fig. 7. It is obvious that higher implantation energy will result in a deeper location of the peak of the dopant concentration. At the same time, the lateral scattering profile is also wider with higher implantation energy. The shorter effective channel length and lightly doped channel result in a larger ON-state current and lower V_{th} for 800-23. For 800-13, a lot of the dopants are not implanted into the channel, but remain in the ARC layer, and the channel is only doped for the upper half. To confirm the reason for the insufficient leakage current suppression, the transfer characteristics of 600-13 and 600-23N are also compared. As shown in Fig. 6(b), for 600-13, the GIDL leakage current is larger than 600-23N, despite the effective channel length of 600-13 being shorter than 600-23N, which results in a larger ON-state current and smaller V_{th}. This result indicates that the poor GIDL control in 600-13 is due to shallow implantation rather than the BG period or effective channel length, which suggests that the back-interface conduction [13] is not well controlled. Therefore, it is necessary to adjust the implantation energy to fully cover the depth of the channel. As the implantation energy also affects the lateral scattering profile, to prevent a lateral short circuit of the BG lines and get enough implantation depth at the same time, the BG period and thickness of the related layers must be carefully designed.

C. Effect of the Aspect Ratio

The exposure ratio in one period also affects the performance of BG-SPC TFTs. The transfer characteristics of 600-23/600-23N and 80-23/80-23N are shown in Fig. 8(a) and (b), respectively. For 600-nm period BG lines, the exposure ratio in one period plays a very important role. As previously discussed and shown, for small period BG lines, the lateral scattering may result in a short circuit of the BG lines. The poor ON/OFF ratio of sample 600-23 is caused by the lateral scattering of dopants. The advantages of using BG are clearly observed in 600-23N, although the ON-state current is not as large as 600-23 due to the longer effective

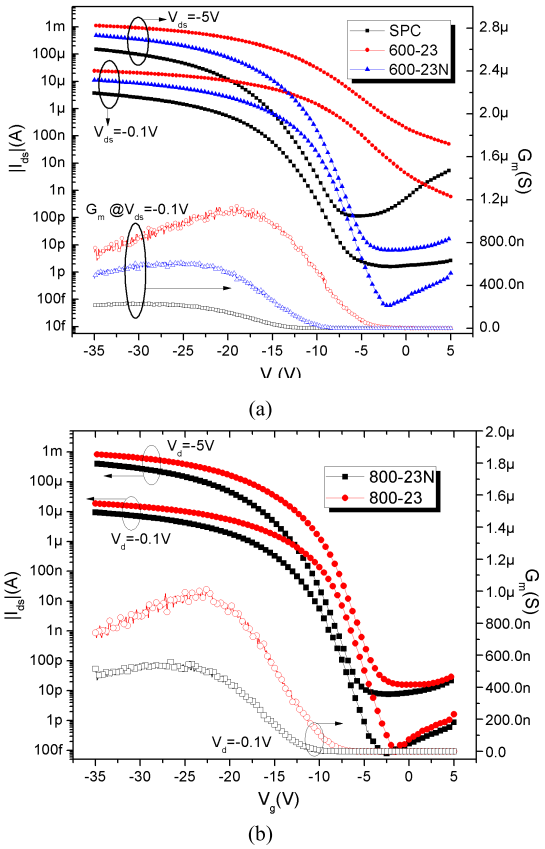

Fig. 8. Transfer characteristics of BG-SPC TFTs with different aspect ratio. (a) 600-23 and 600-23N and (b) 800-23 and 800-23N.

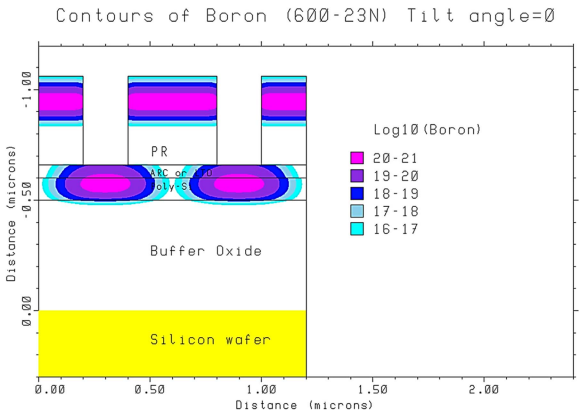

Fig. 9. Contour plots of dopant distribution for sample 600-23N.

channel length. The simulation result of the dopant distribution for 600-23N is shown in Fig. 9. Compared with the previous plot of 600-23, shown in Fig. 4(a), partially lightly doped short channels can be formed in 600-23N. As shown in Fig. 8(b), samples 800-23 and 800-23N can both work properly with BG structures, which indicate that the lateral scattering of dopants is not the critical parameter for 800-nm period BG lines at an implantation energy of 23 keV. Of course, 800-23 demonstrates larger ON-state current and lower V_{th} due to the shorter effective channel length. The GIDL currents for 800-23 and 800-23N are comparable, as the implantation depths of the BG dopants are the same for these two samples.

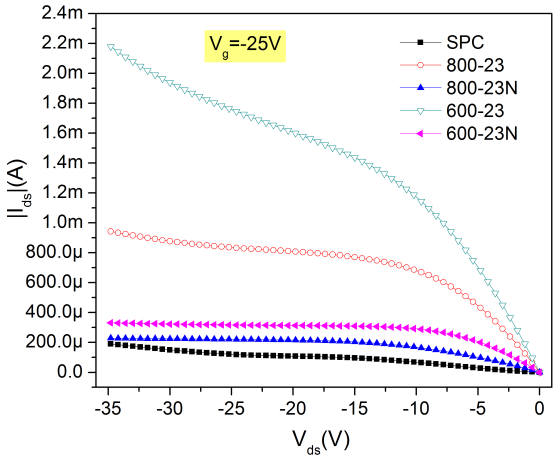

Fig. 10. Output characteristics of the SPC and BG-SPC TFTs.

The output characteristics of the BG TFTs using the same implantation condition but different BG configurations measured at $V_g = -25$ V is plotted in Fig. 10, together with the output characteristics of the reference SPC TFT ($W/L = 24/10$ μm on the layout). The kink effect is related to the drain electric field. The main cause of the kink effect is impact ionization near the drain at high drain voltage. This effect is also observed in Silicon On Insulator (SoI) devices due to the same floating body in TFTs and SoI transistors. However, in poly-Si TFTs, the carriers trapped at the grain boundaries can be freed under the high drain electric field, which makes the situation much more serious.

From Fig. 10, kink effect is observed in the reference SPC TFTs (see the black curve with square marks). Short-channel effects result in enhanced kink effect. However, the inherent multijunction structure in a BG TFT helps reducing the electric field near the drain depletion region and relieving the kink effect. Although the subchannel lengths of the BG TFTs are in submicrometer scale, for sample 600-23N, 800-23N, and 800-23, the kink effect is still sufficiently suppressed. This improvement coincides with the GIDL reduction observed in the transfer characteristics of these BG TFTs. For sample 600-23, the enhanced kink effect is observed and it is due to the over-scaled subchannel length and ion scattering during the implantation process. This observation is also in accordance with the transfer characteristics of 600-23 shown in Fig. 3.

IV. Conclusion

The BG SPC TFTs were fabricated and characterized. Larger ON-state current and ON/OFF current ratio, lower V_{th}, and sharper SS were achieved in BG TFTs, making use of the merits of the grain size effect, short channel effect, and drain electric field relief. The influence of different process parameters on the device performance was investigated. It was shown that the period of the BG lines, exposure ratio, and the BG implantation energy all affect the performance of BG TFTs from different aspects. The BG period is expected to be made small to increase the number of BG lines inside the channel as long as the BG lines are not shorted through lateral scattering. The optimized BG SPC TFTs are promising for advanced AM applications.

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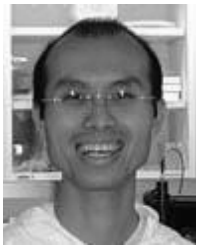

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